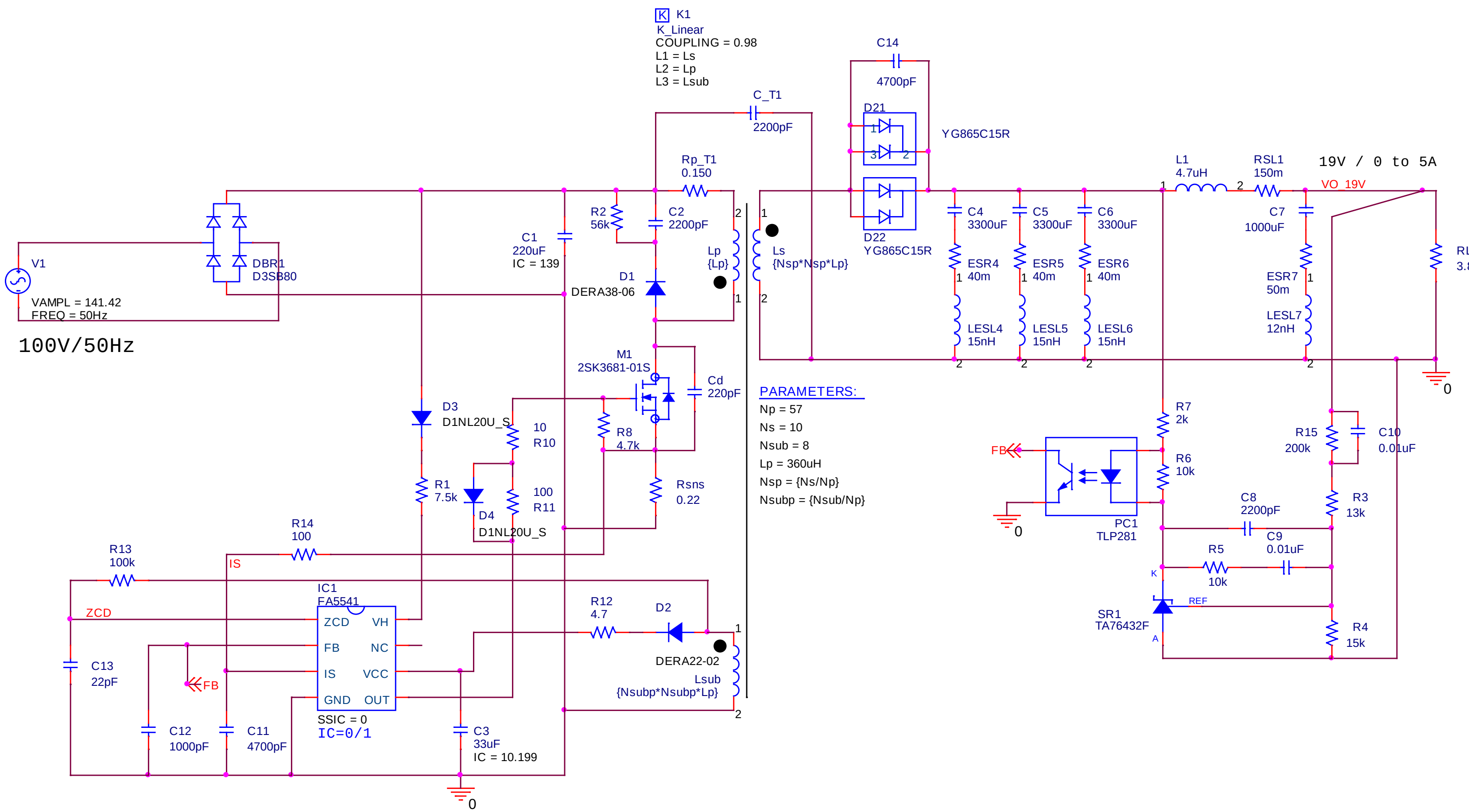
Design Kit

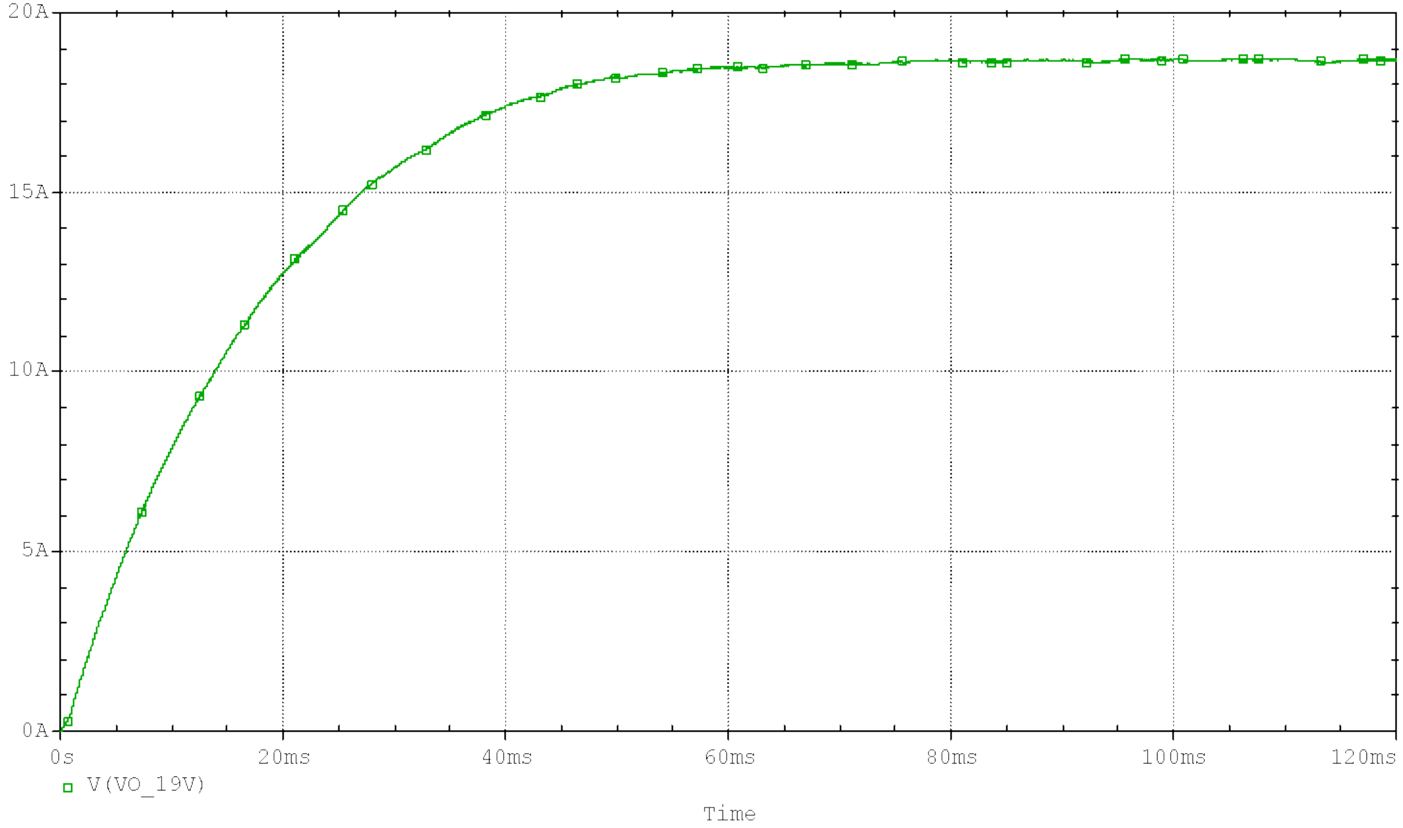
Quasi-Resonant Switching Power Supply using FA5541

Contents

1.Quasi-Resonant Switching Power Supply 19V/5A

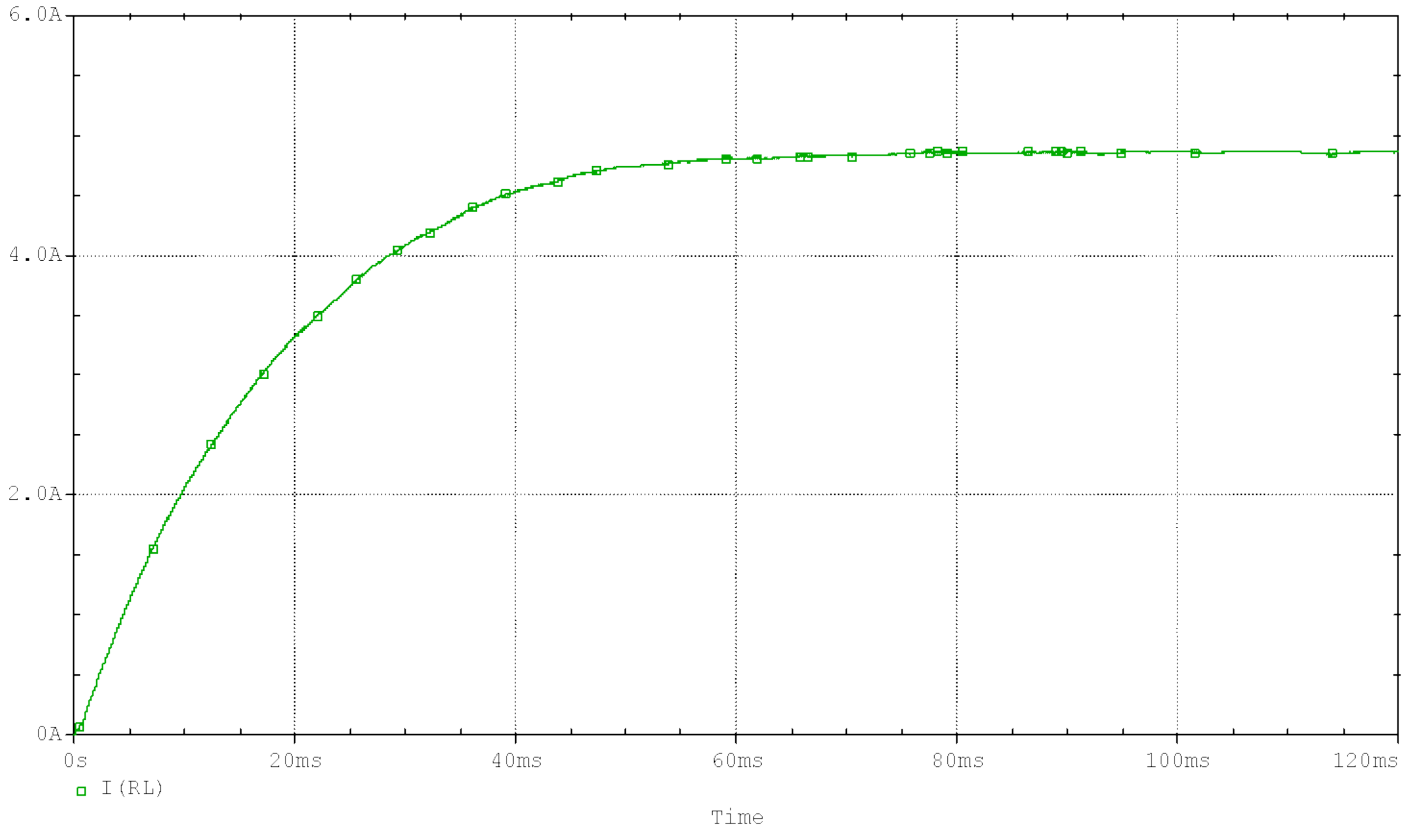


1.1 Output voltage



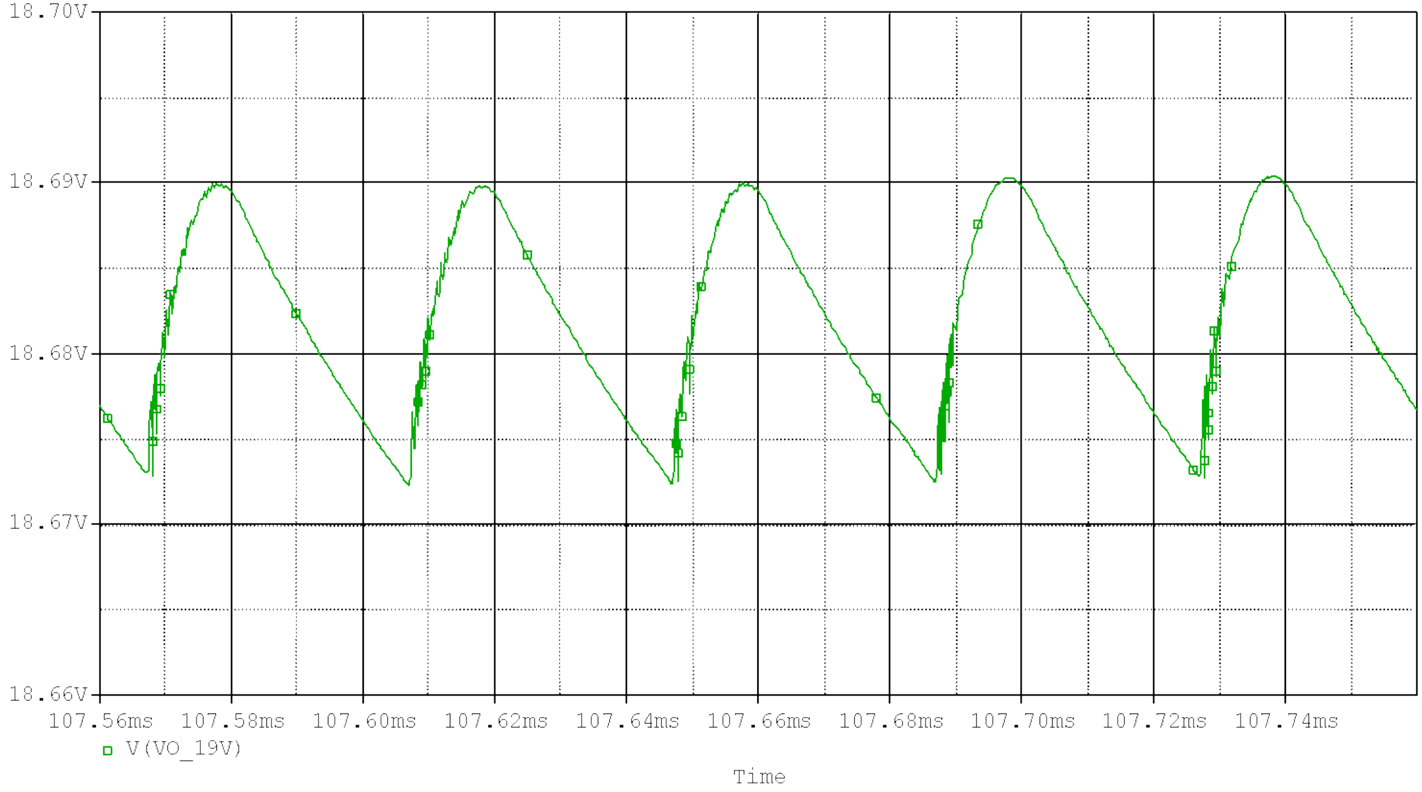
- Simulation result confirming that the output voltage would be 19 Volt at 5-A load. The result also shows that the circuit need 60ms to reach steady state.

1.2 Output current



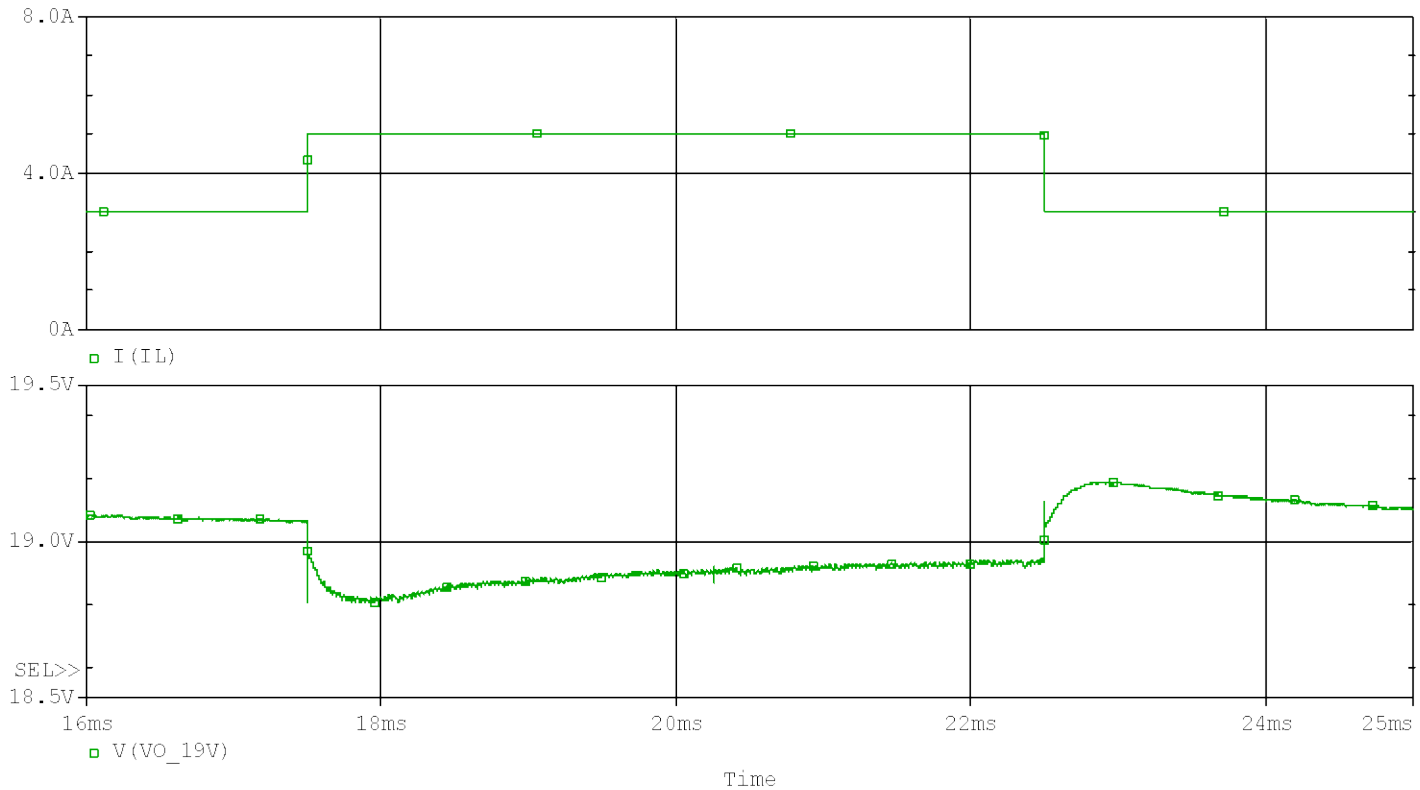
- Simulation result confirming that the output current would be 5 Amp. The result also shows that the circuit need 60ms to reach steady state.

1.3 Output ripple voltage



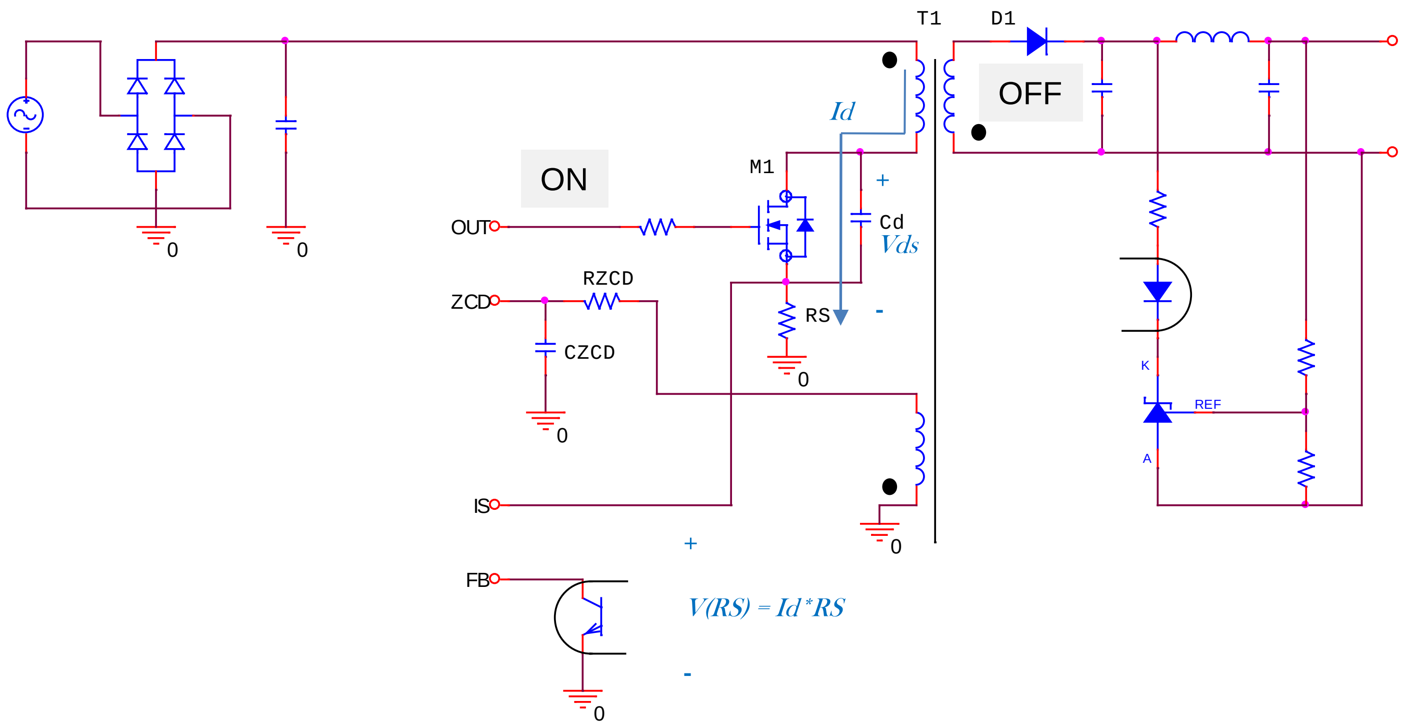
- Simulation results shows the output ripple voltage at maximum current load (approximately 17.5mV_{P-P}).

1.4 Step-load response



- Simulation results shows waveform of the output voltage responding to stepping current 3/5A.

2.Basic operation of switching power supply using FA5541



- Power supply using FA5541 is switching using self-excited oscillation.
- When IC turns the MOSFET ON ,drain current Id (primary current of T1) begins to rise from zero.
- V(IS pin) is voltage-converted from the Id current.

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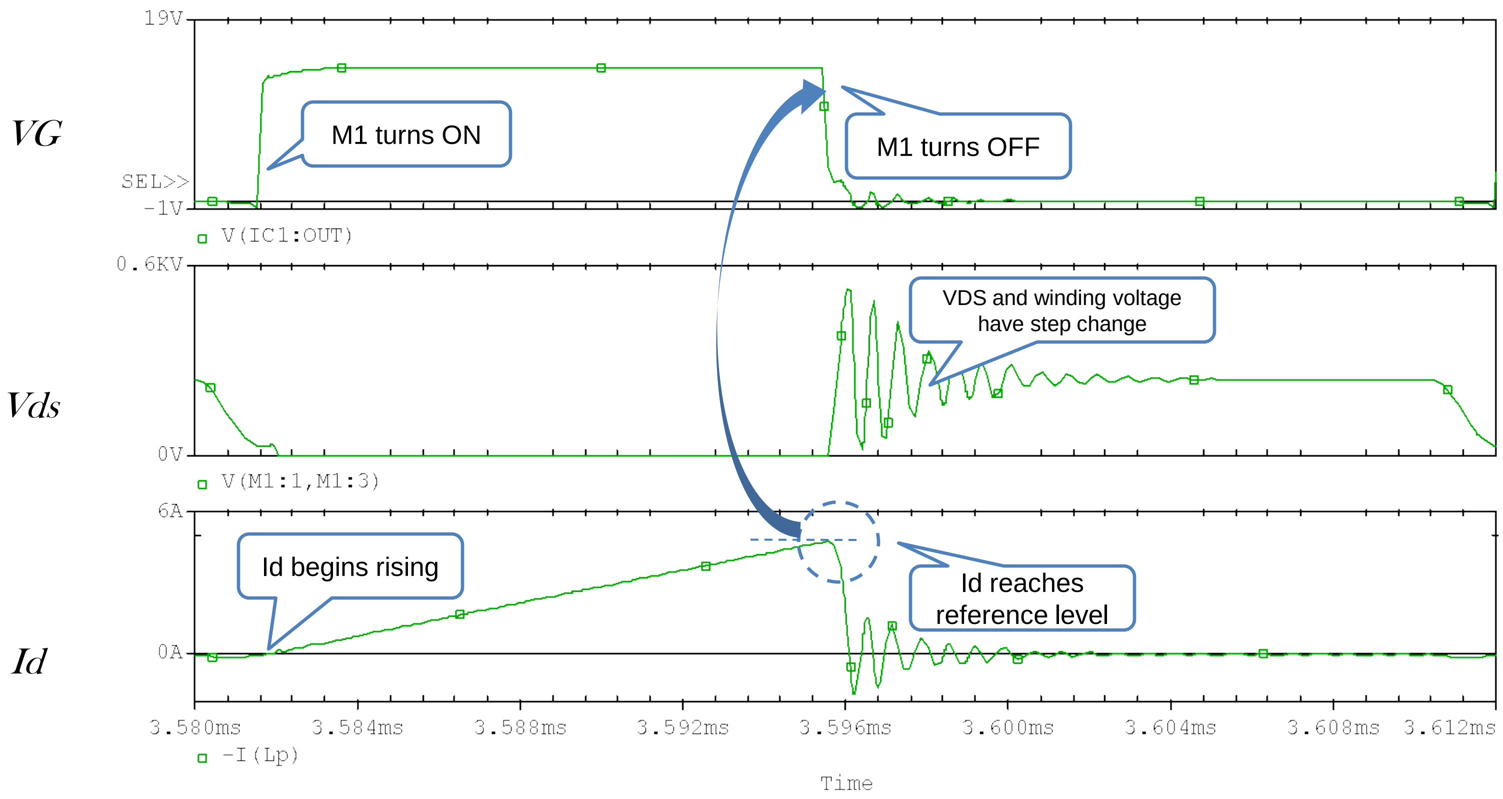
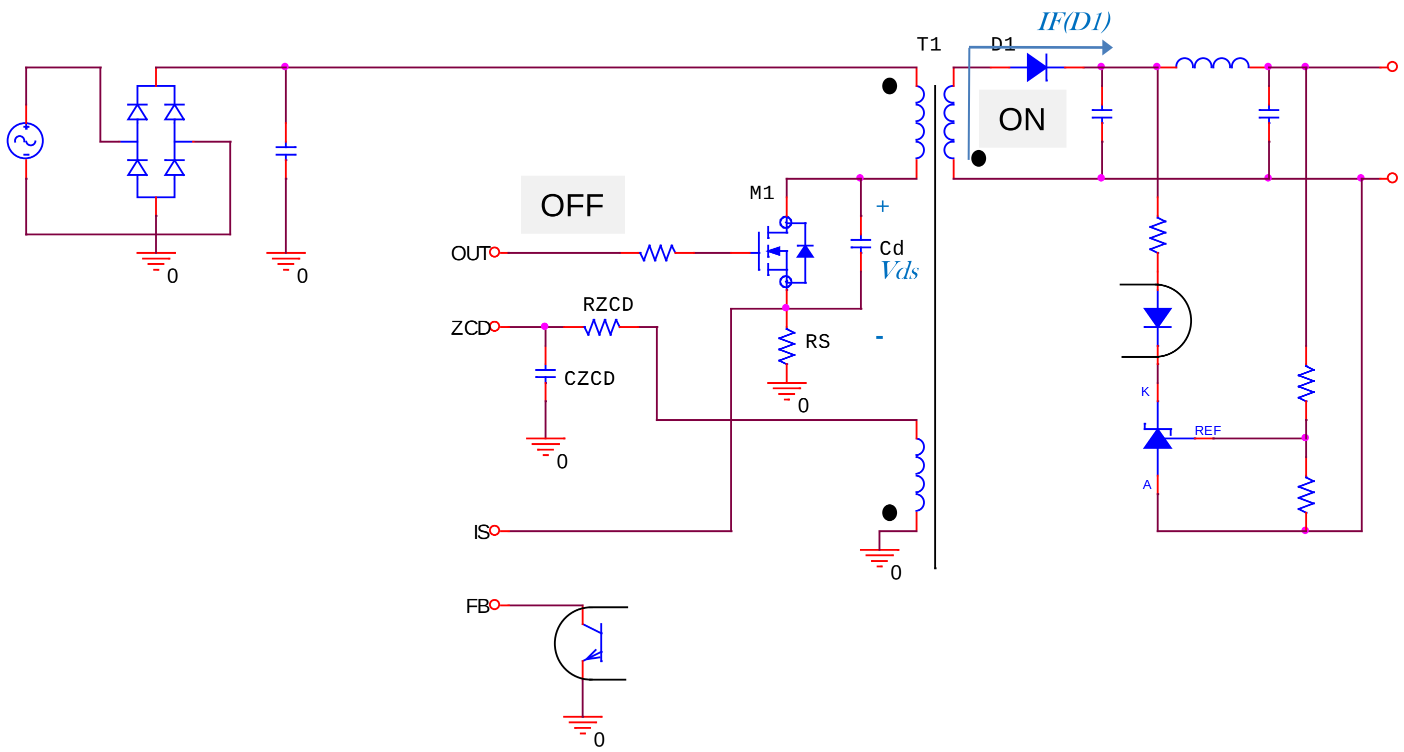


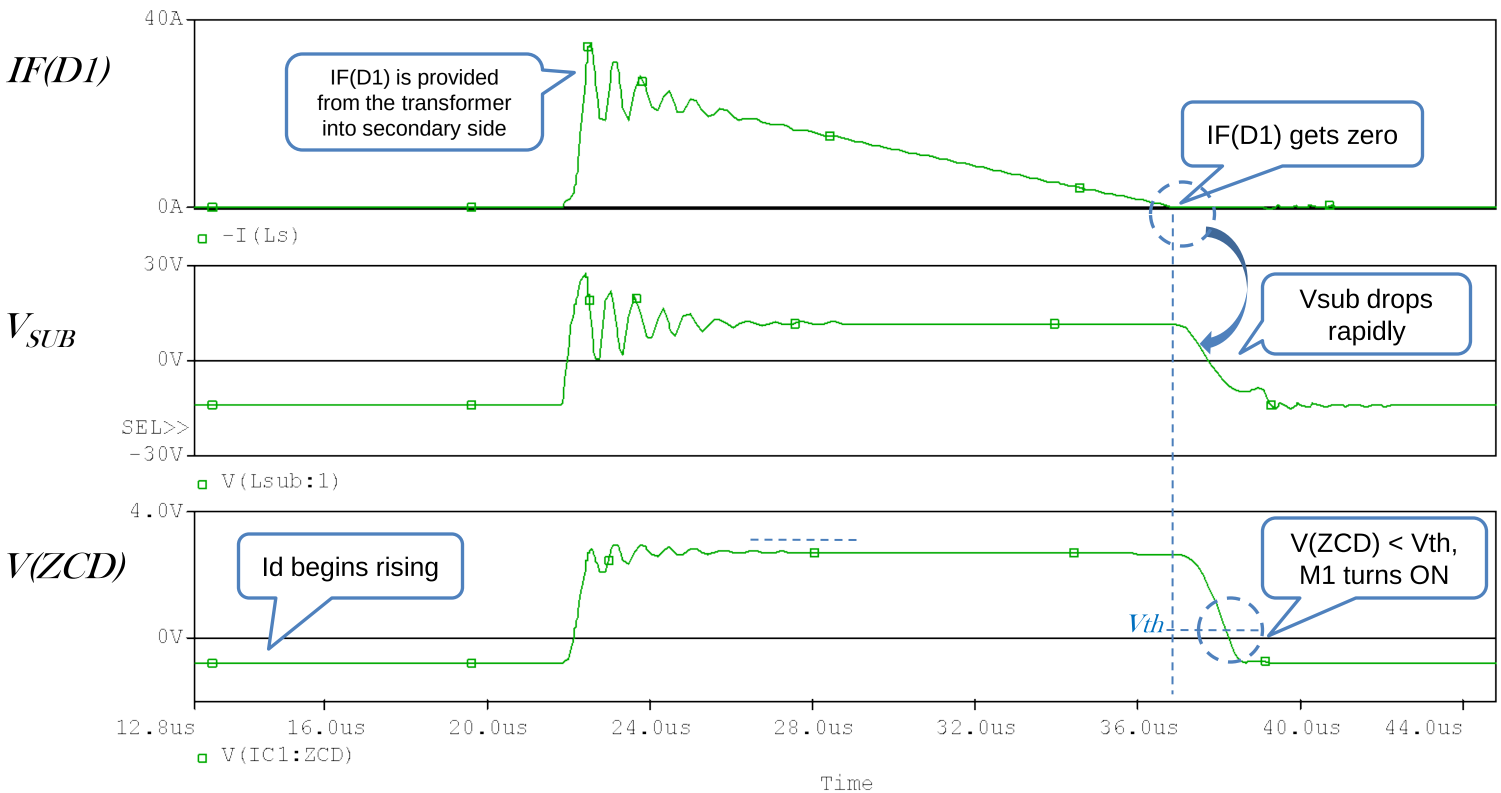
- When Id reaches the reference level, FA5541 will turn M1 OFF

2.Basic operation of switching power supply using FA5541



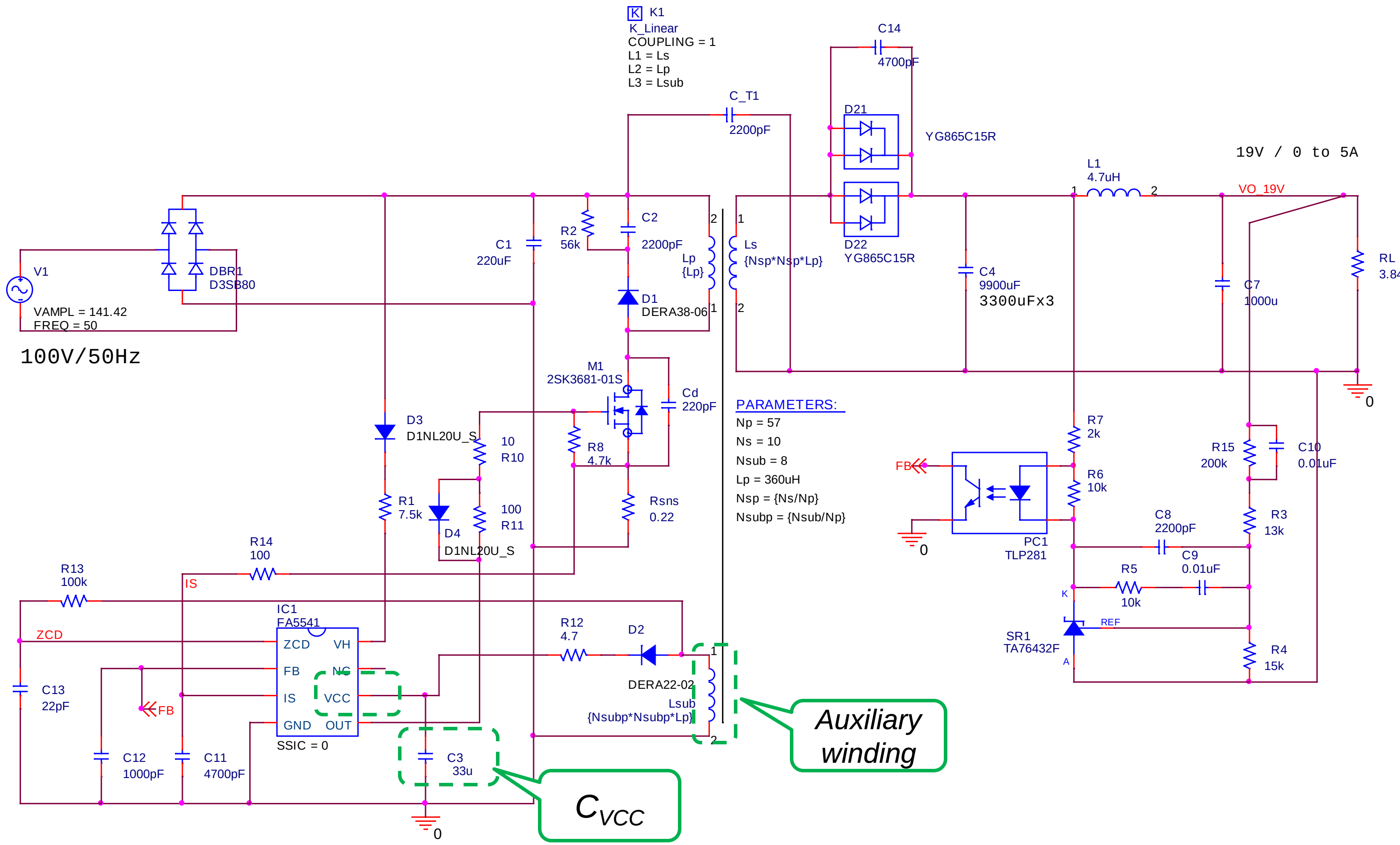
- When M1 turns OFF ,and the winding voltage of the transformers has step change and IF(D1) is provided from the transformer into secondary side.

2.Basic operation of switching power supply using FA5541



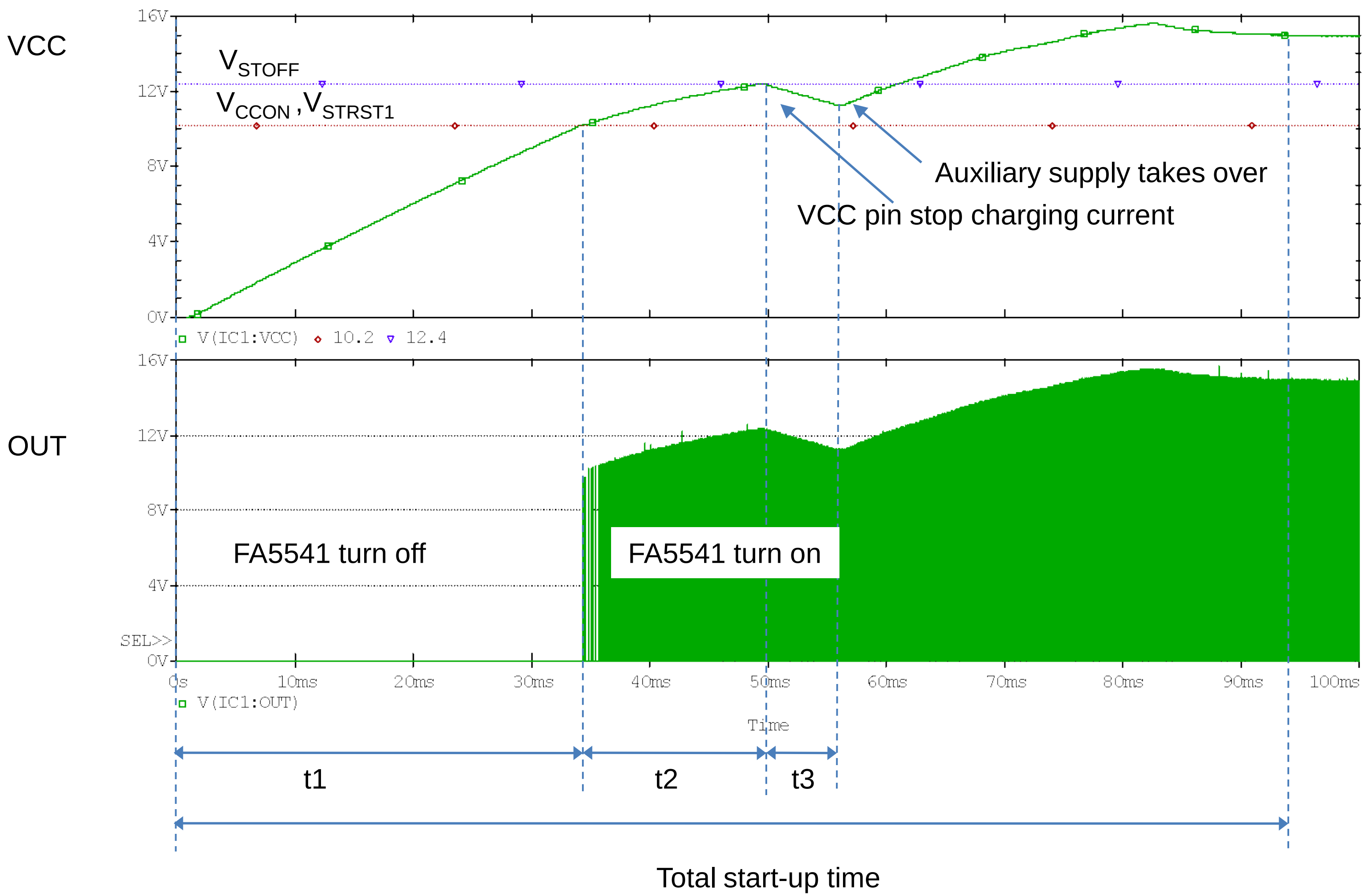
- When IF(D1) gets zero, Vds drops rapidly due to resonance of transformers inductance and Cd. At the same time Vsub also drops rapidly.
- When V(ZCD) < Vth(of valley detection) ,FA5541 turns M1 ON again

3.Start-up sequence simulation



※ No parasitic elements and no initial condition is set

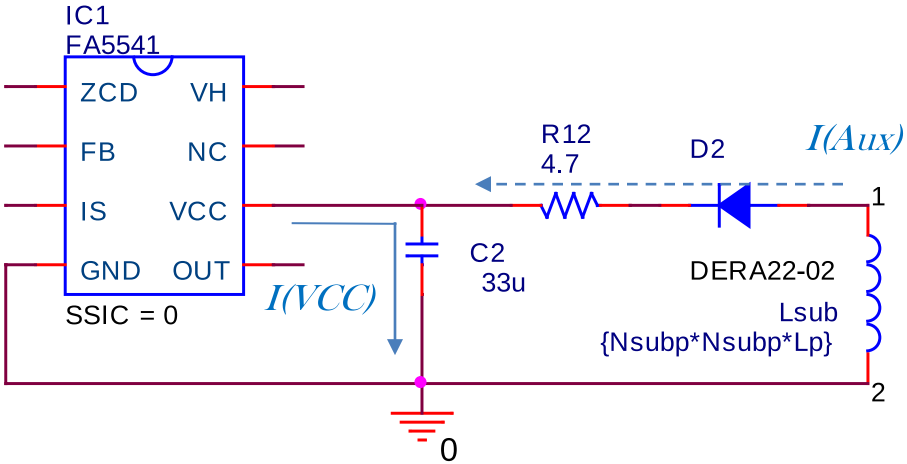
3.Start-up sequence simulation



3.Start-up sequence simulation

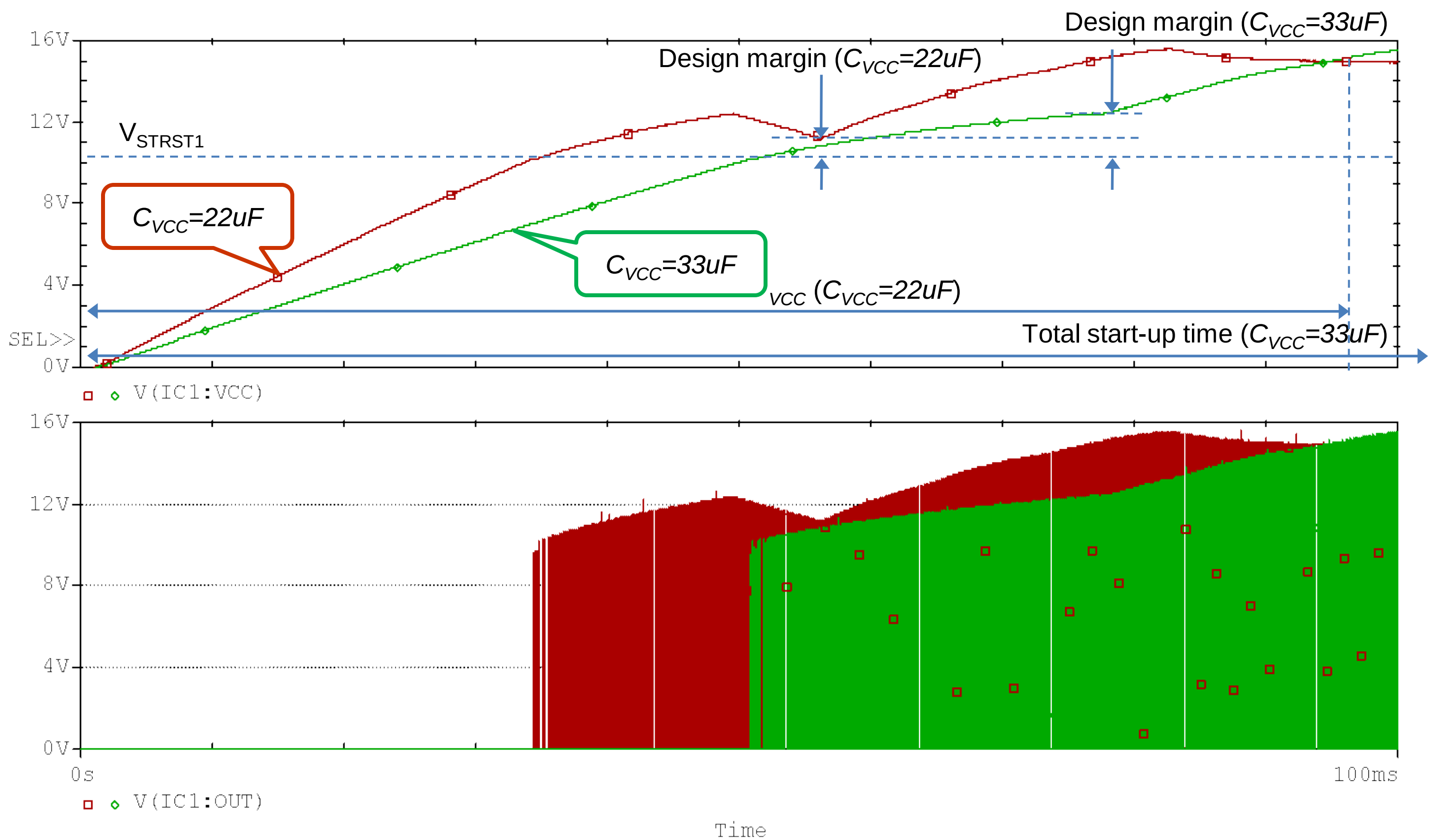
FA5541 under voltage lockout (UVLO) characteristics (VCC pin)

- ON threshold voltage: V_{CCON} = 10.2V
- Startup circuit shutdown: V_{STOFF} = 12.4V
- Startup circuit reset voltage: V_{STRST1} = 10.2V



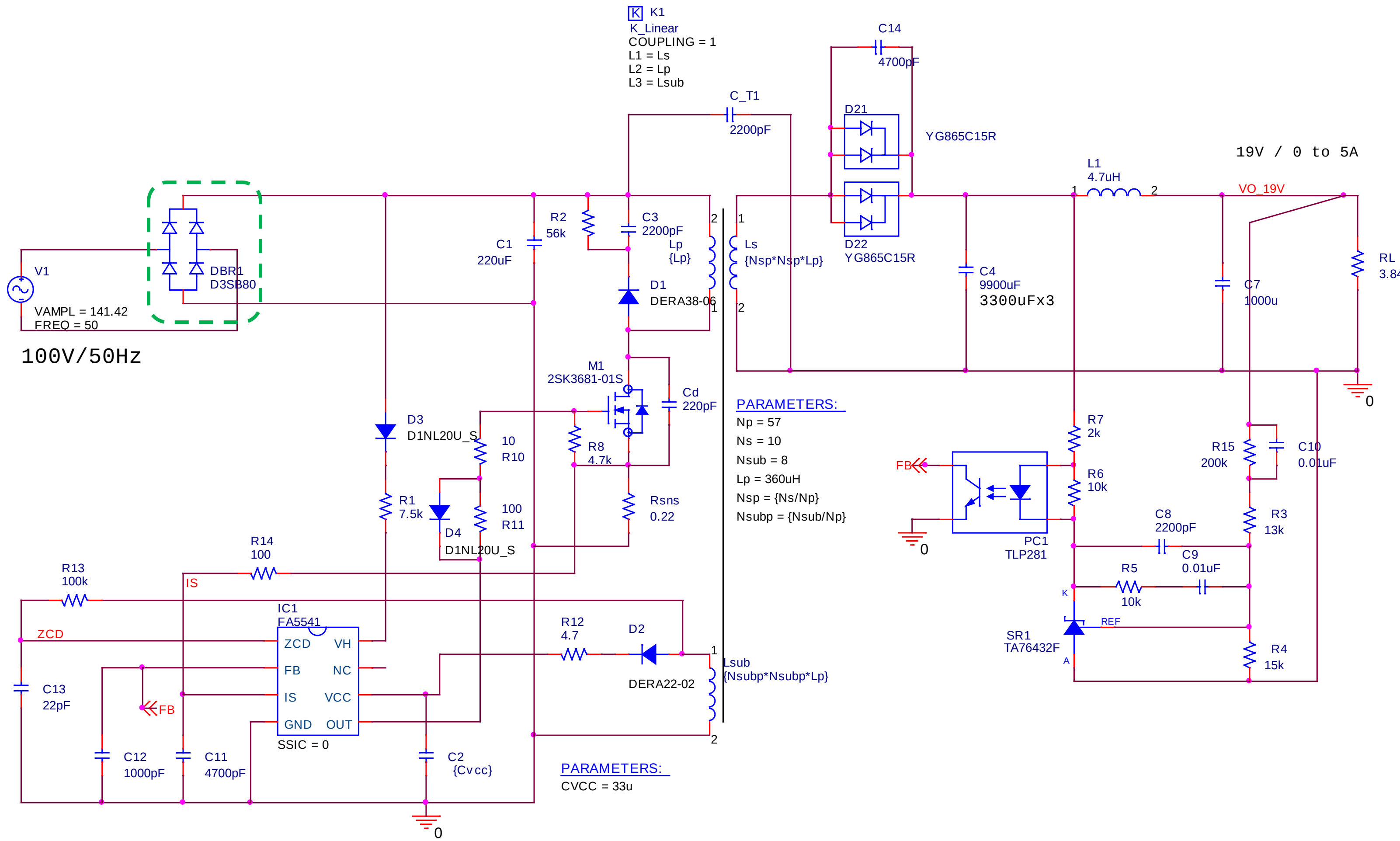
t1,t2: $V_{CC} < V_{STOFF}$,startup circuit turns on ,VCC pin charges capacitor C_{VCC} (C2).
t2: V_{CC} reaches V_{CCON} ,FA5541 is turned on
t3: after V_{CC} reaches V_{STOFF} ,startup circuit turns off , V_{CC} decreases until Auxiliary supply takes over.

3.Start-up sequence simulation



- the simulation result shows the tradeoff between Total start-up time and Design margin, which is the difference of V(VCC) and VSTRST1 when the auxiliary winding takes over from the IC startup circuit.
- 33uF-CVCC is selected for higher Design margin although total start-up time is high.

4.Bridge diode peak current at start-up



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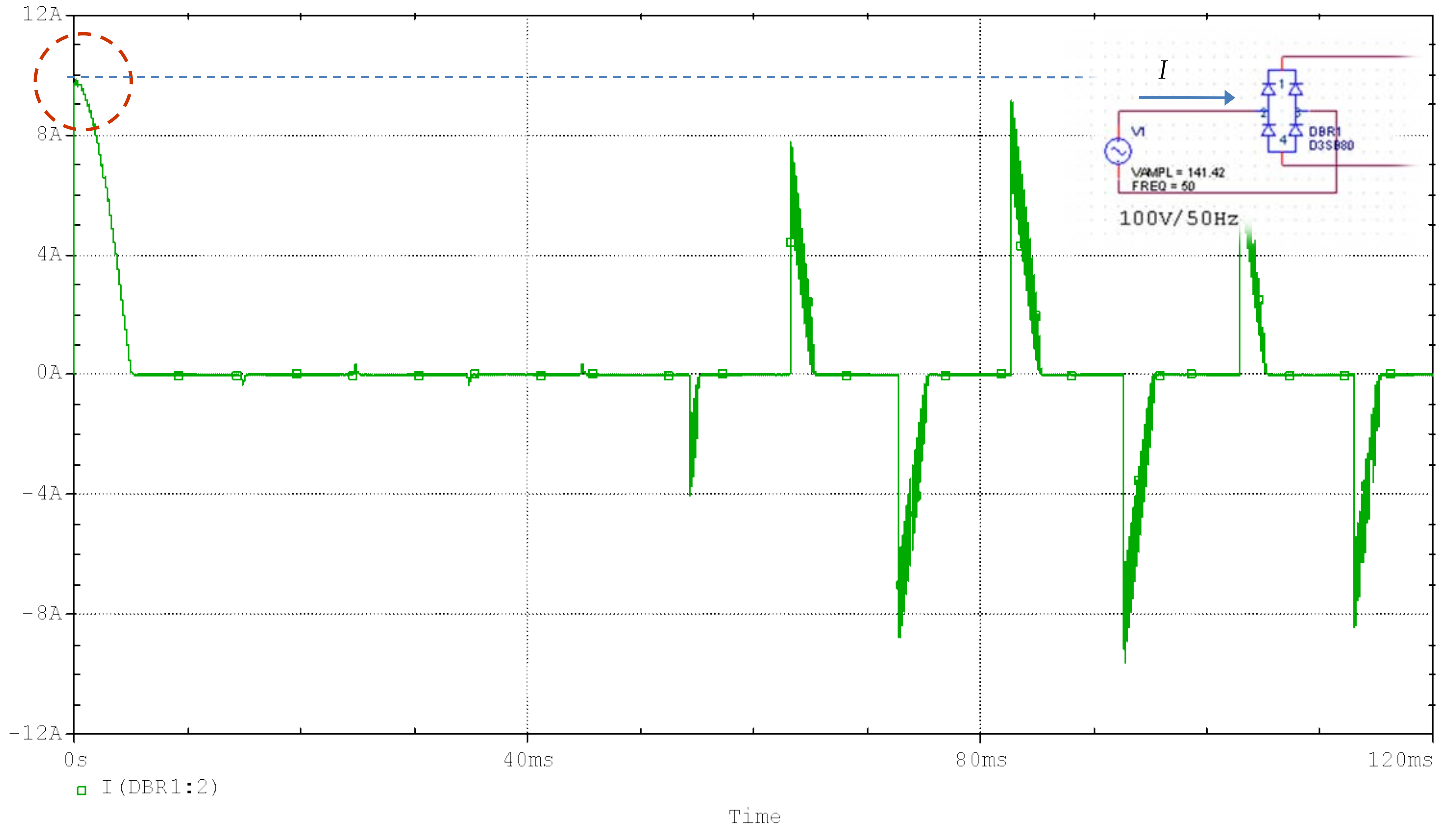
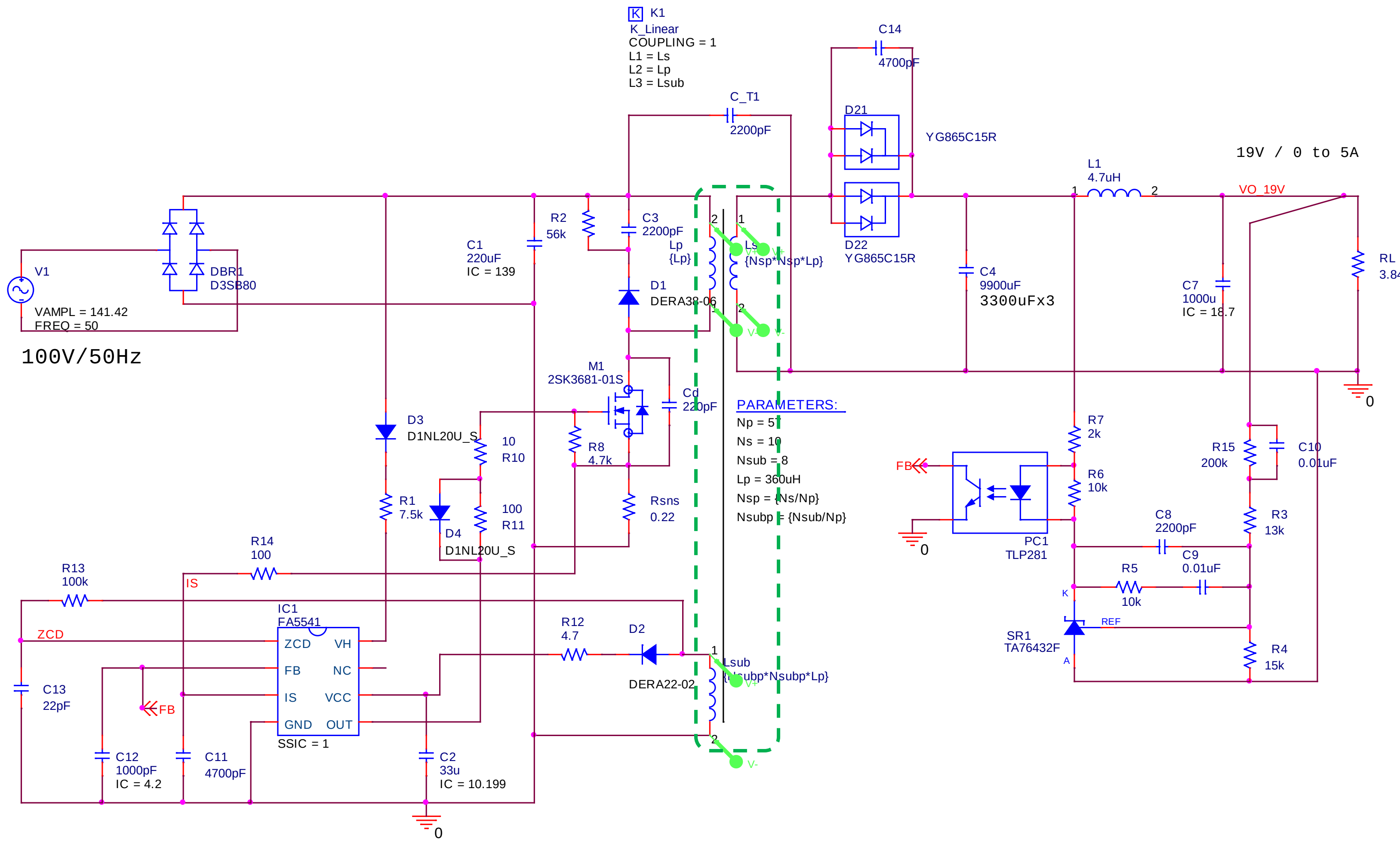
4.Bridge diode peak current at start-up



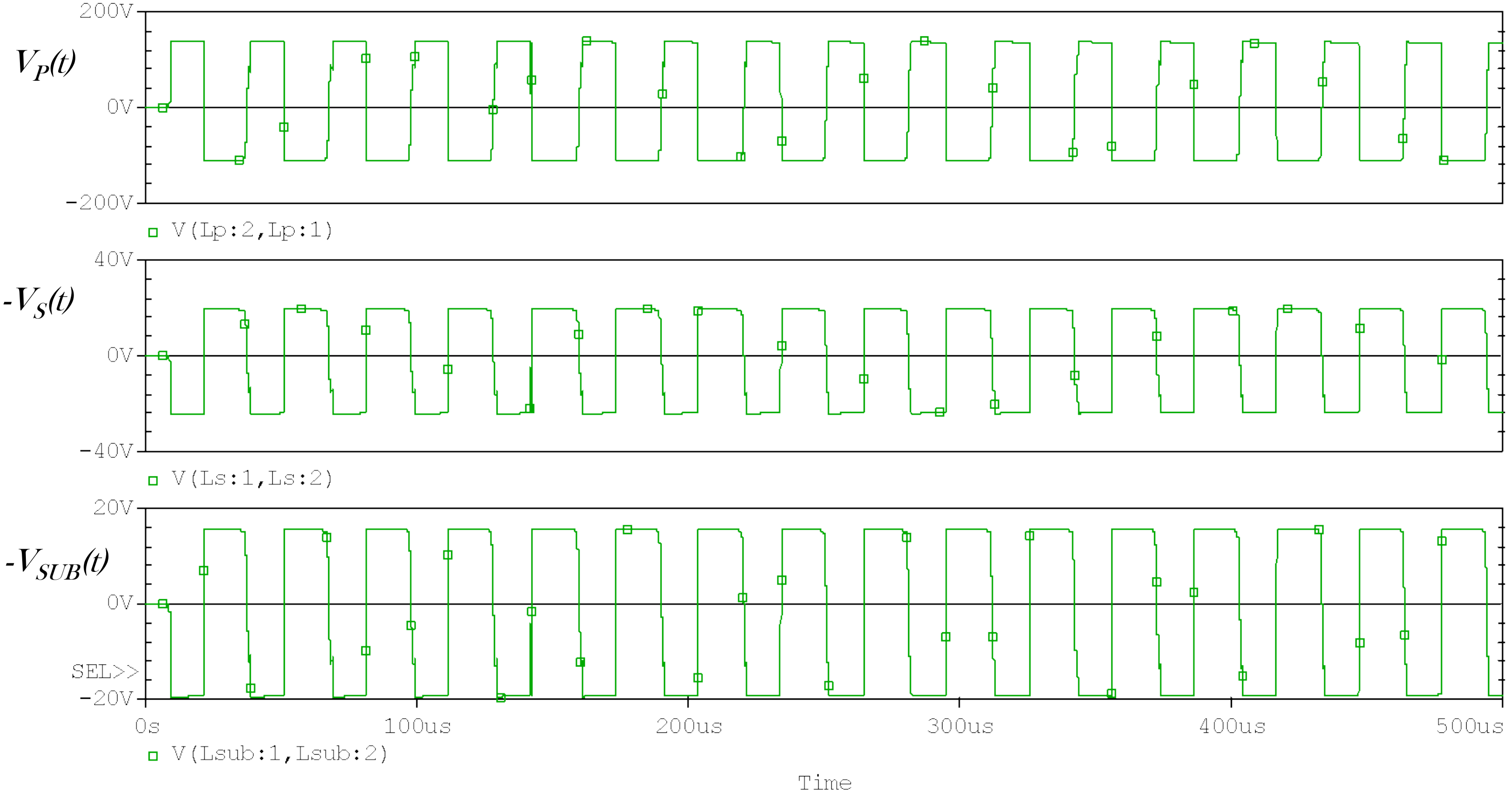
- Simulation result of the current through bridge rectifier diode DBR1 when the power supply is plug to the wall outlet. the peak current is approximately 9.8 which is less than Absolute maximum value IFSM from the datasheet.

5.Transformer



※ No parasitic elements

5.Transformer



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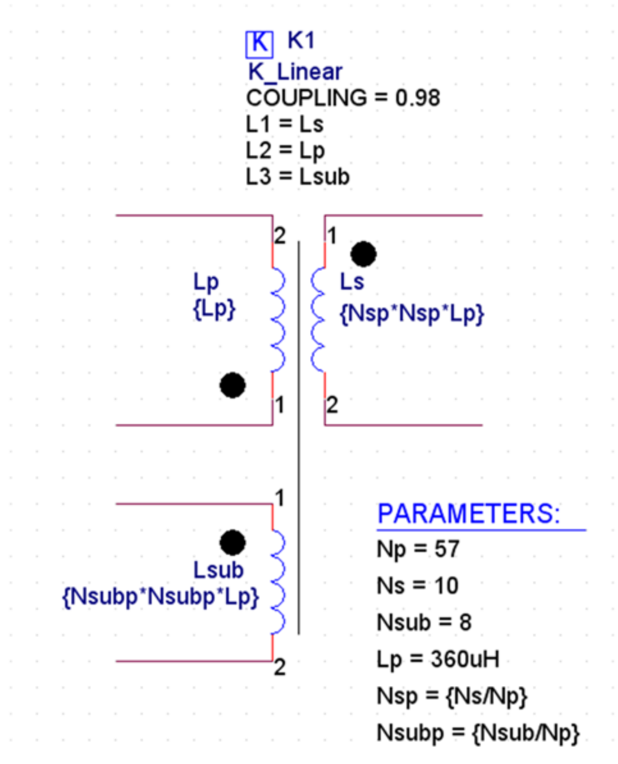


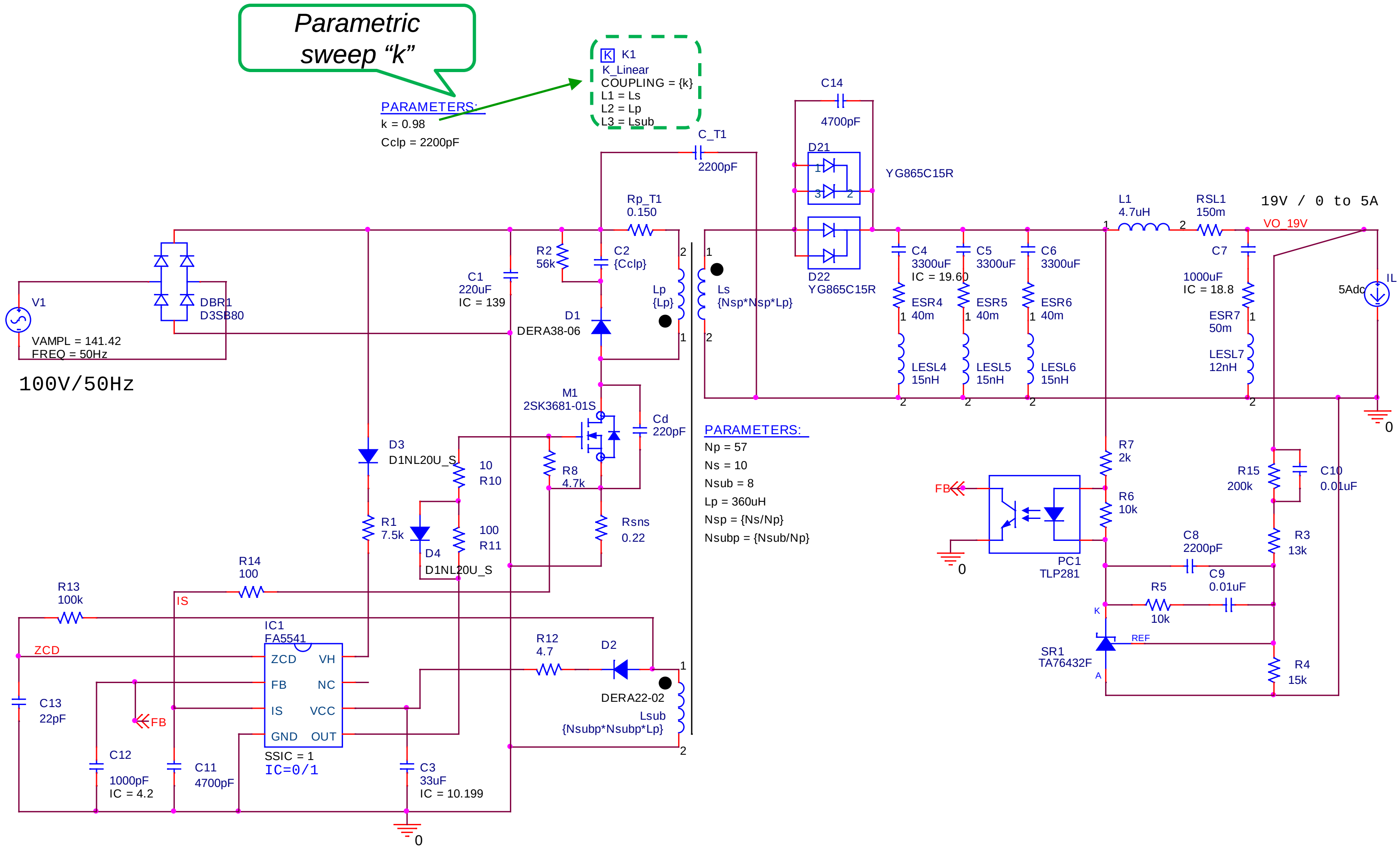
- $L_{leak} = L_P(1-k^2)$
- $L_S/L_P = N^2$

N : winding ratio of the transformer

$$V_S = V_P*(N_S/N_P)$$
$$V_{SUB} = V_P*(N_{SUB}/N_P)$$

- Transformer is modeled by using SPICE primitive k ,the transformer spec is Lp=360uH and Np:Ns:Nsub=57:10:8

6.Transformer leakage inductance



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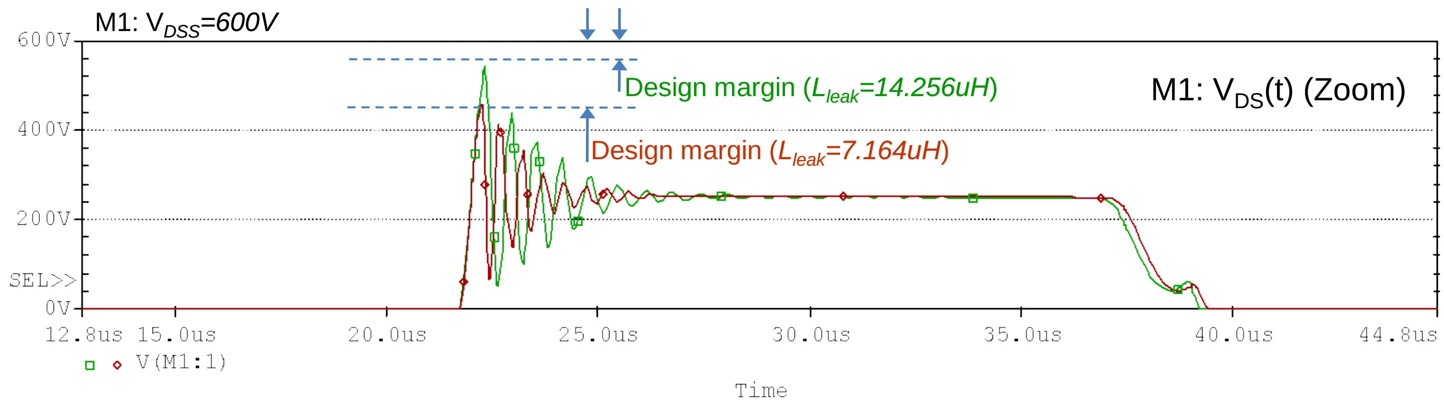
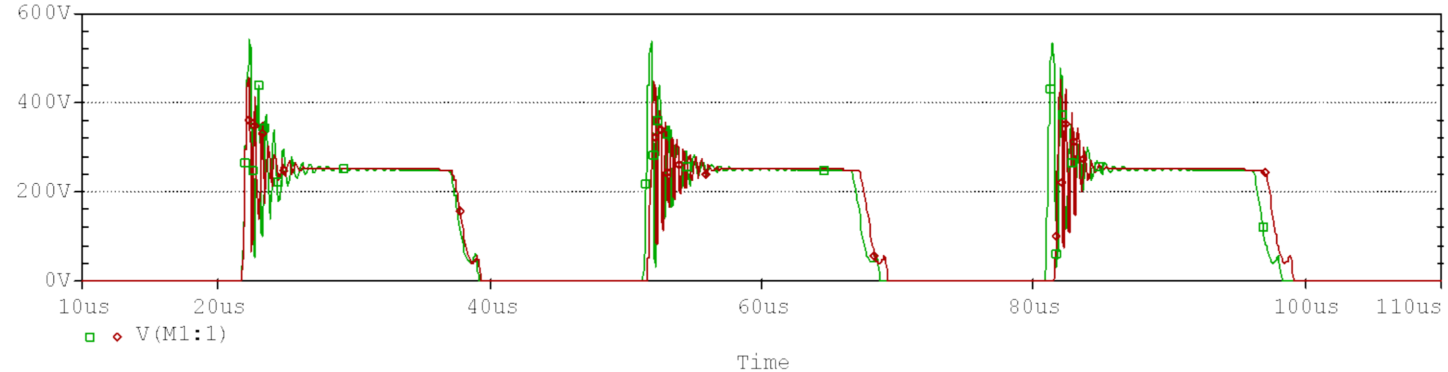
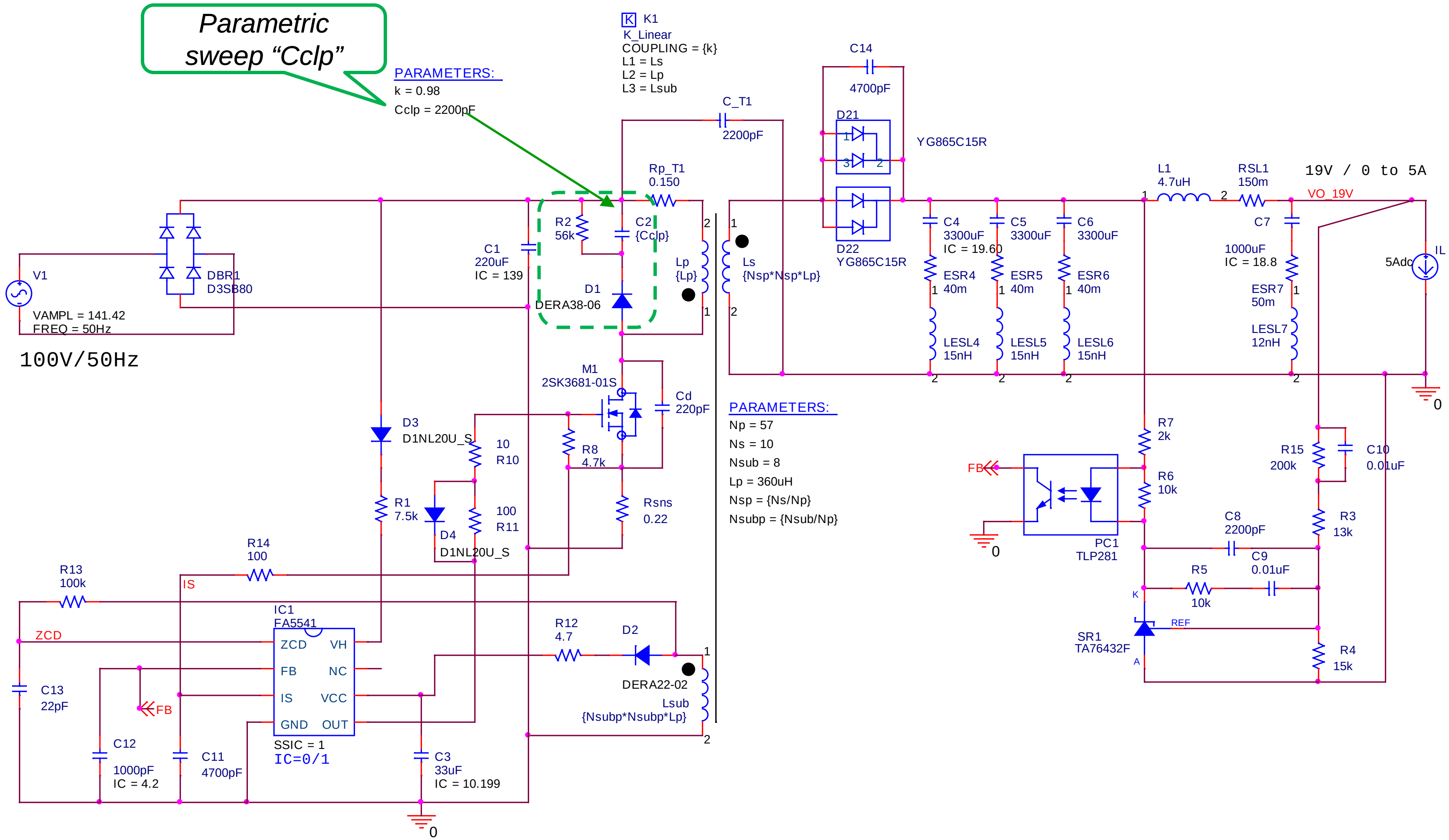


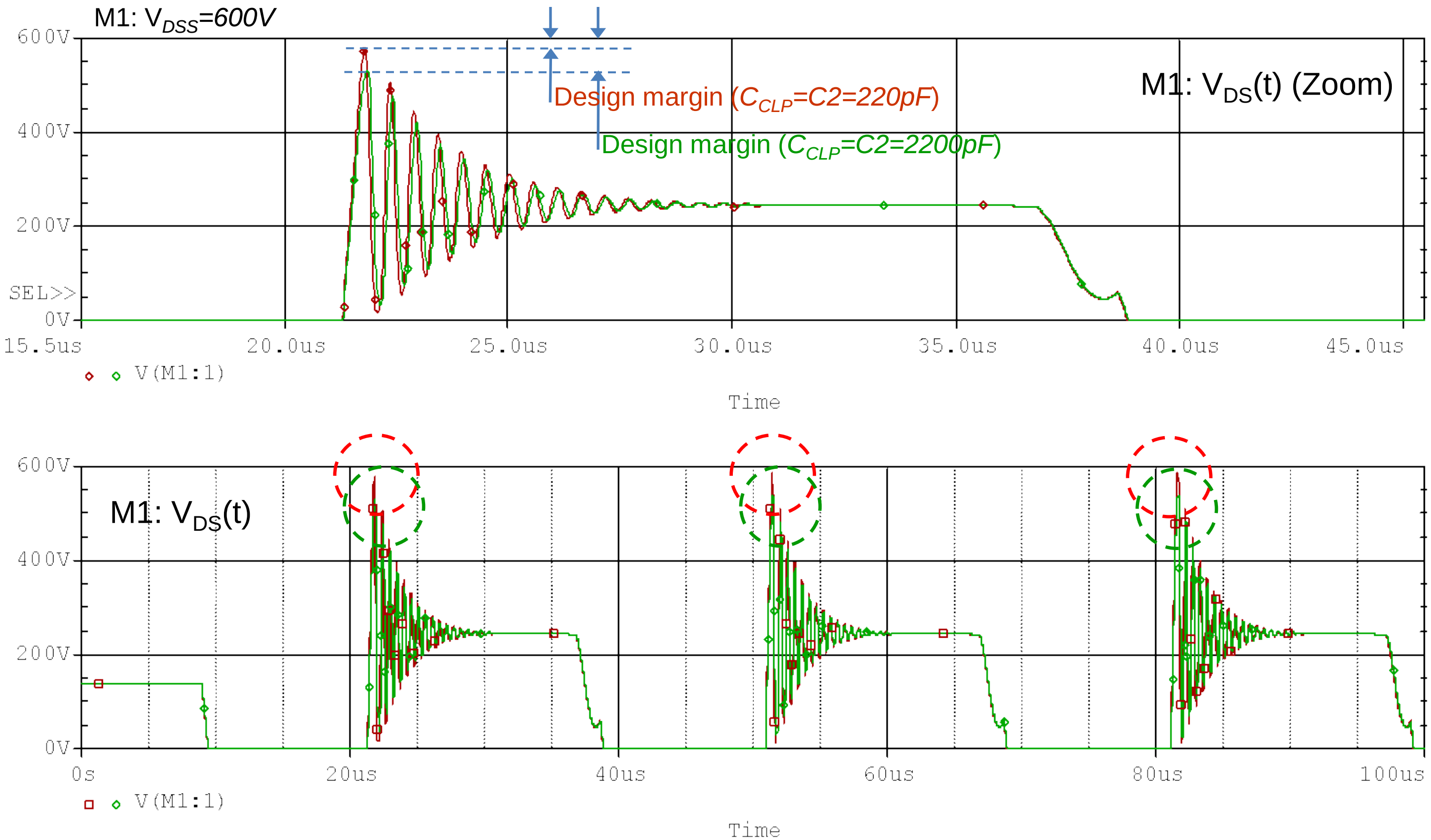


- Transformer model using SPICE primitive k ,leakage inductance: $L_{leak} = L_P(1-k^2)$
- L_P=360uH ,leakage inductance is14.256uH for k=0.98 and 7.164uH for k=0.99
- Check the VDS overshoot voltage versus the transformer leakage inductance.

7.RCD Clamping network

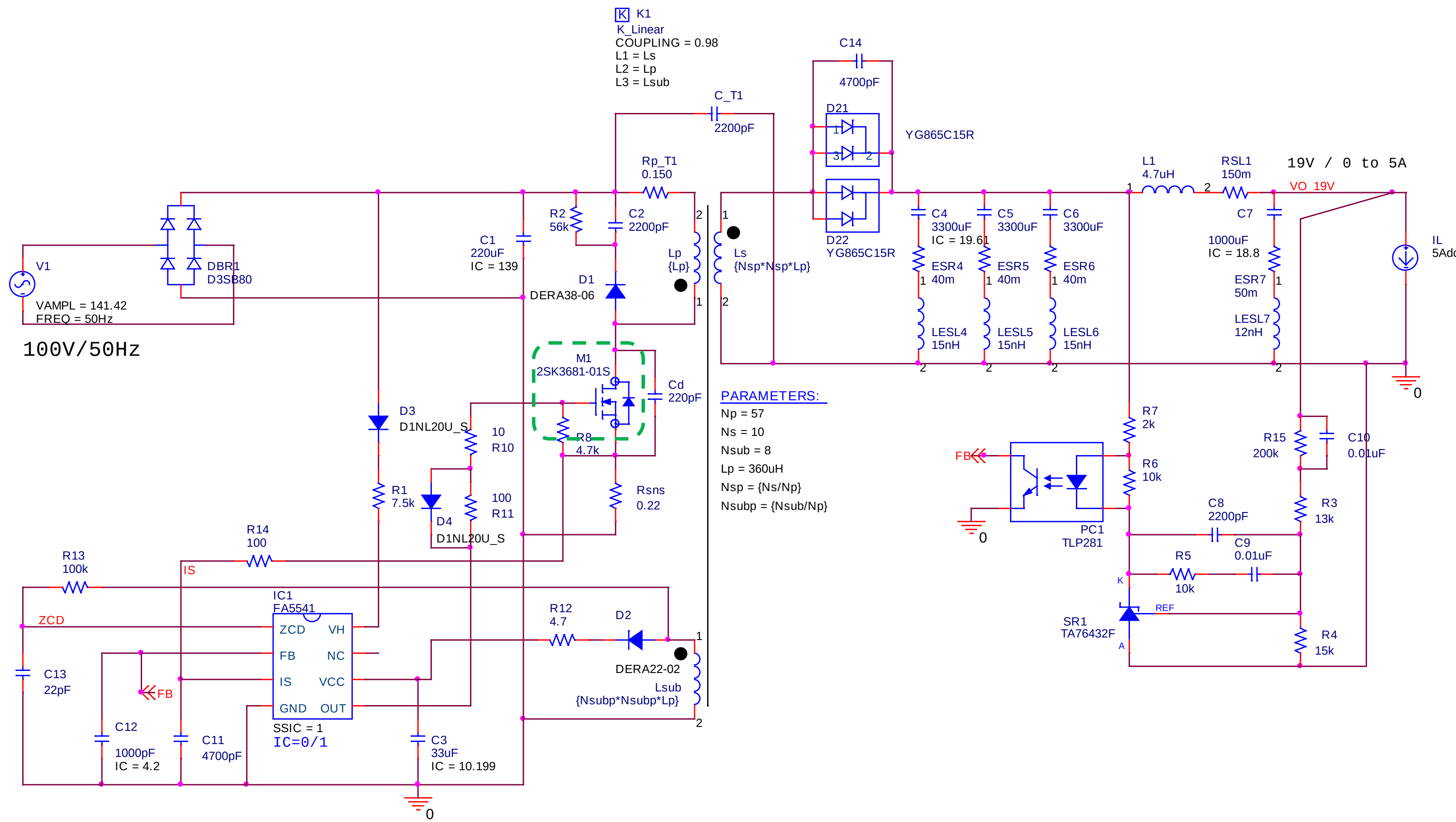


7.RCD Clamping network



- Compare VDS overshoot of the circuit with C_{CLP}(C2) = 220pF and 2200pF ,larger C_{CLP} value get better design margin for MOSFET V_{DS}
- C_{CLP}=2200uF is selected for the better M1: V_{DS} design margin.

8.Power MOSFET switching device



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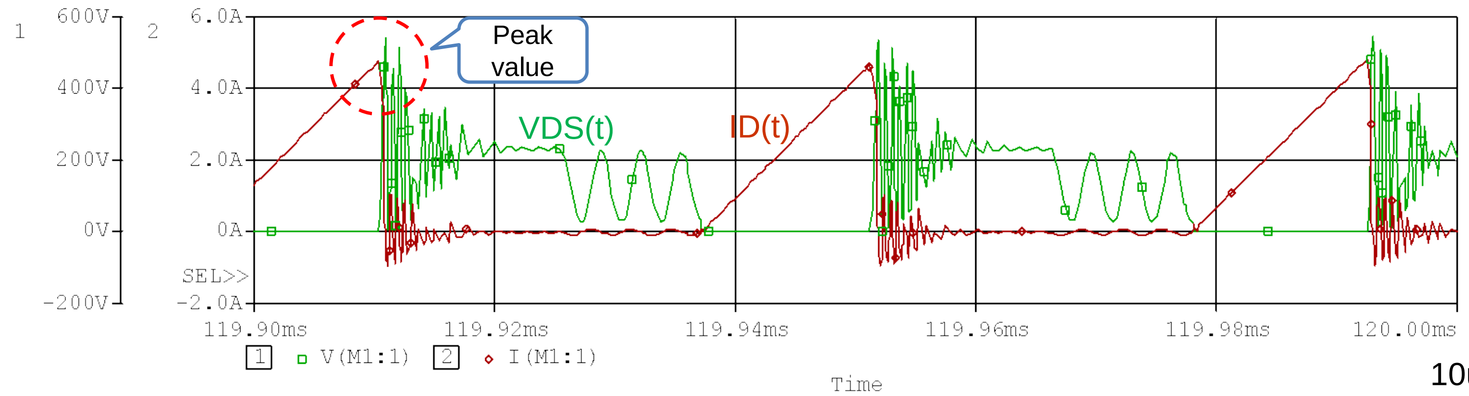
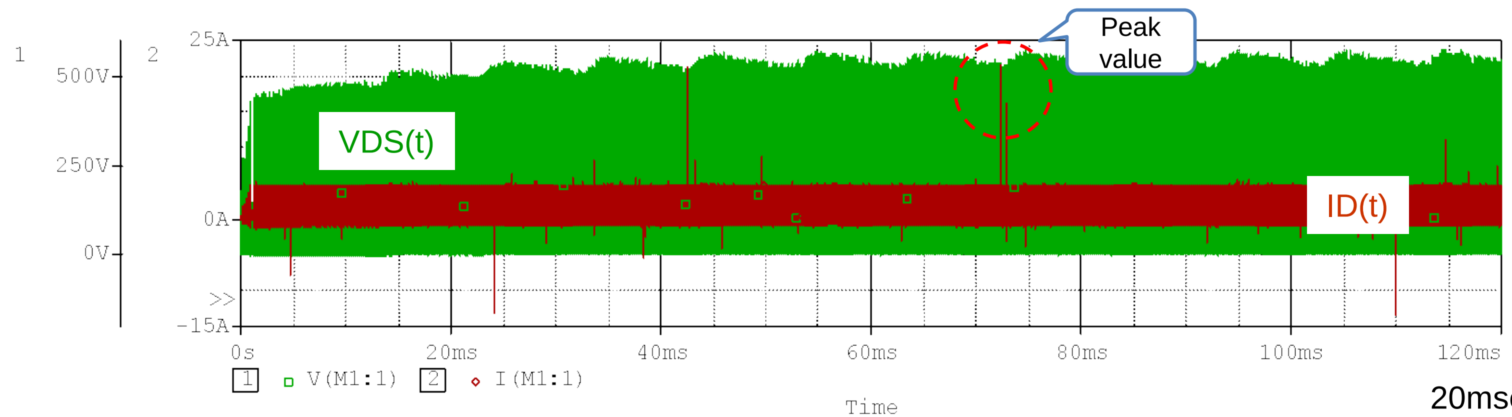


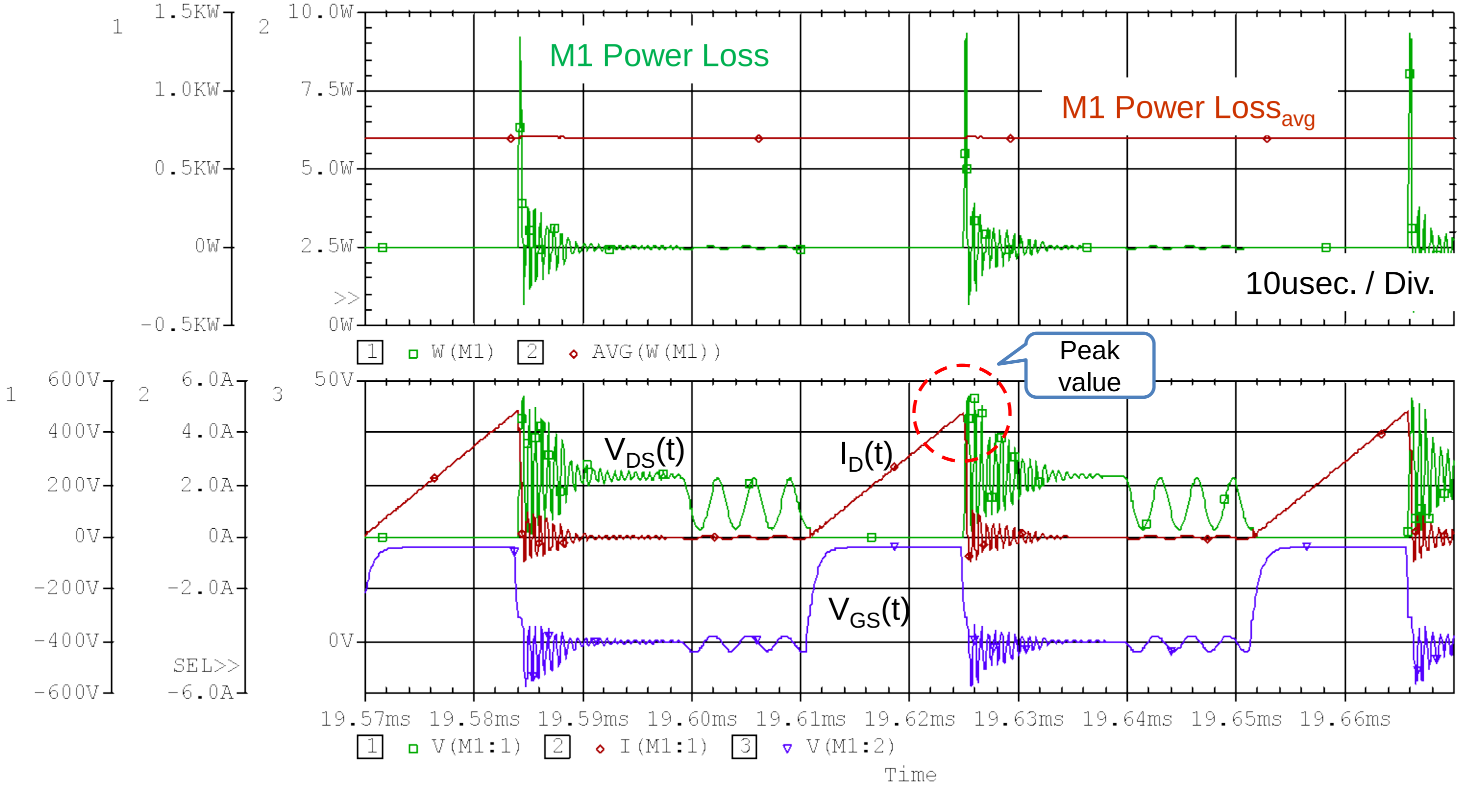
10usec. / Div.



20msec. / Div.

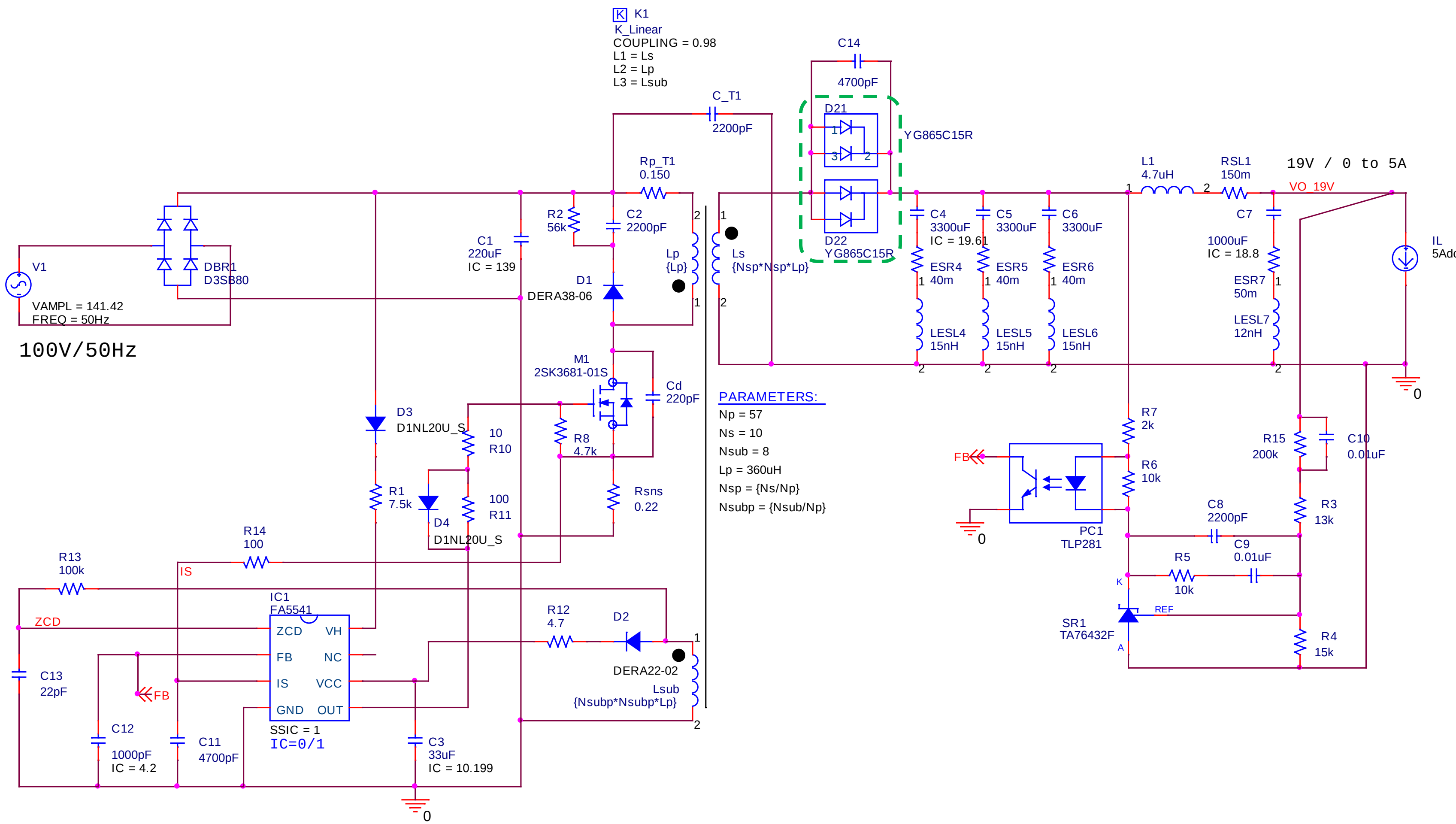
- Simulation results shows the peak value of M1: VDS and ID .

8.Power MOSFET switching device



- Simulation results shows the peak value of MOSFET VDS and ID . Calculated switching power loss and average power loss are also shown

9.Schottky barrier diode D21 and D22 waveforms



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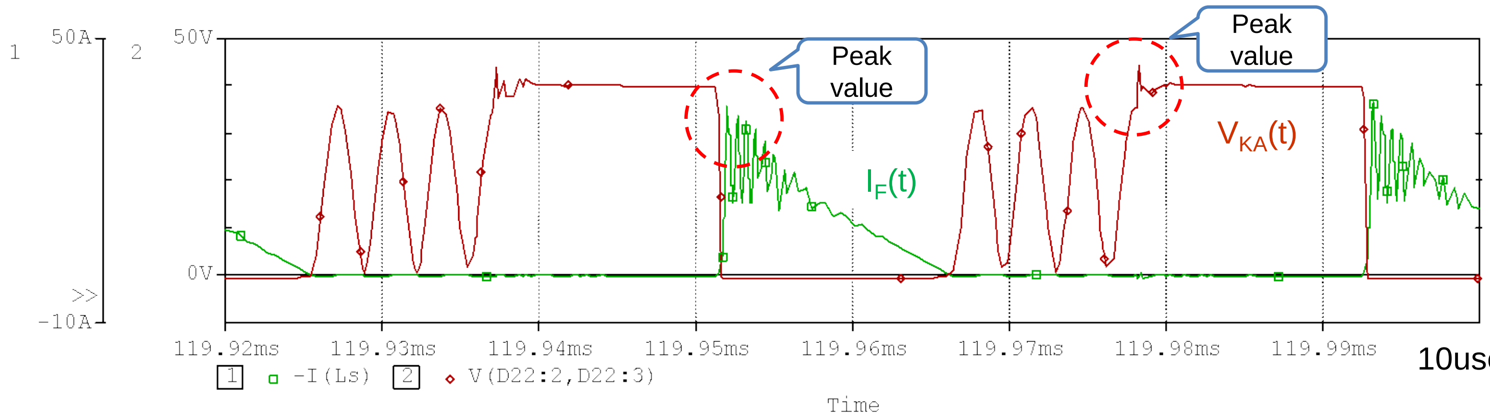
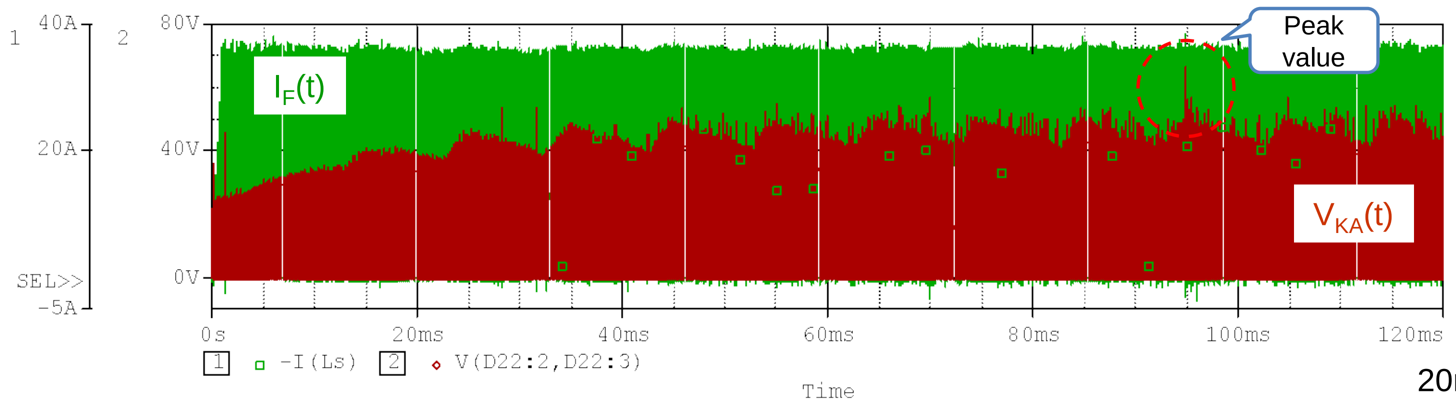


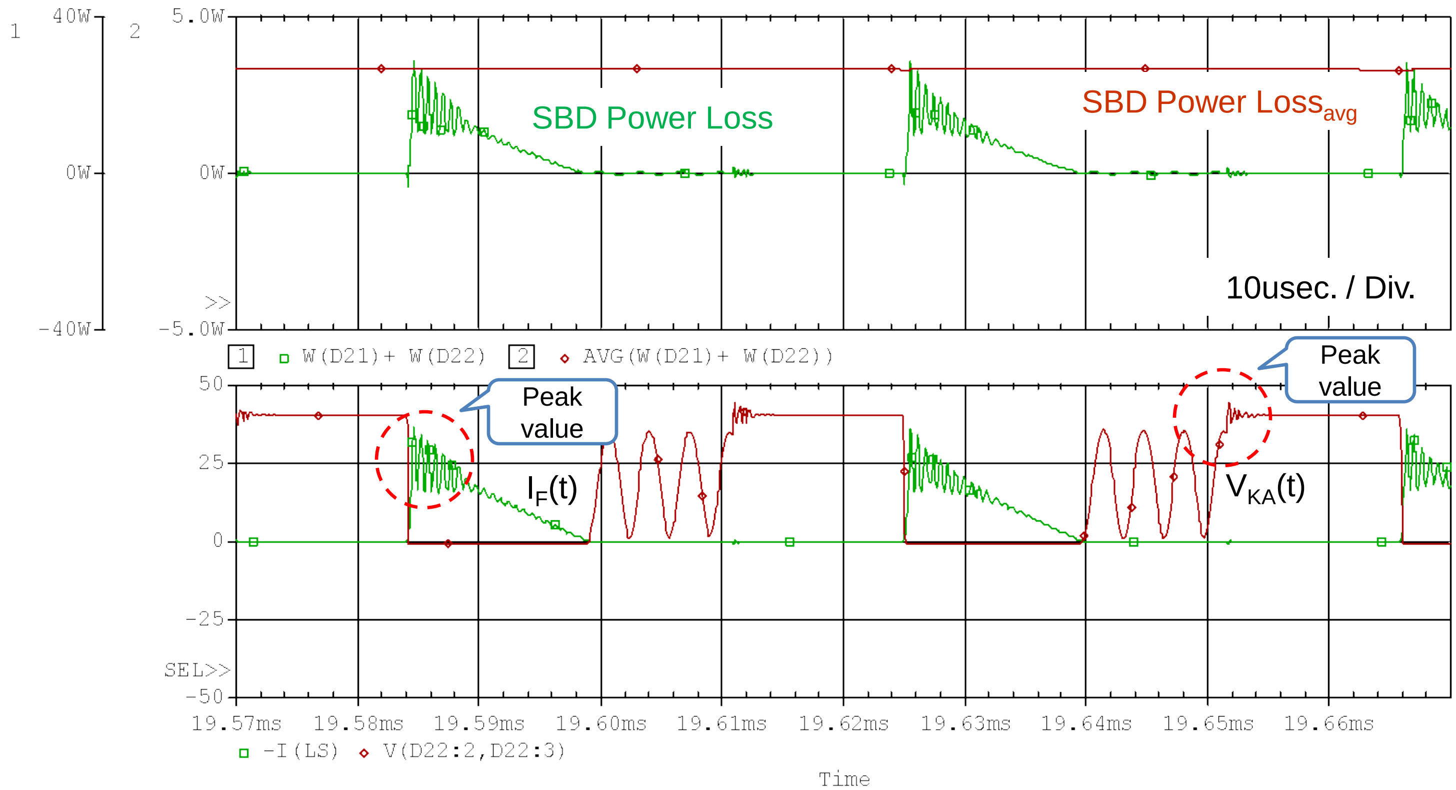
10usec. / Div.



20msec. / Div.

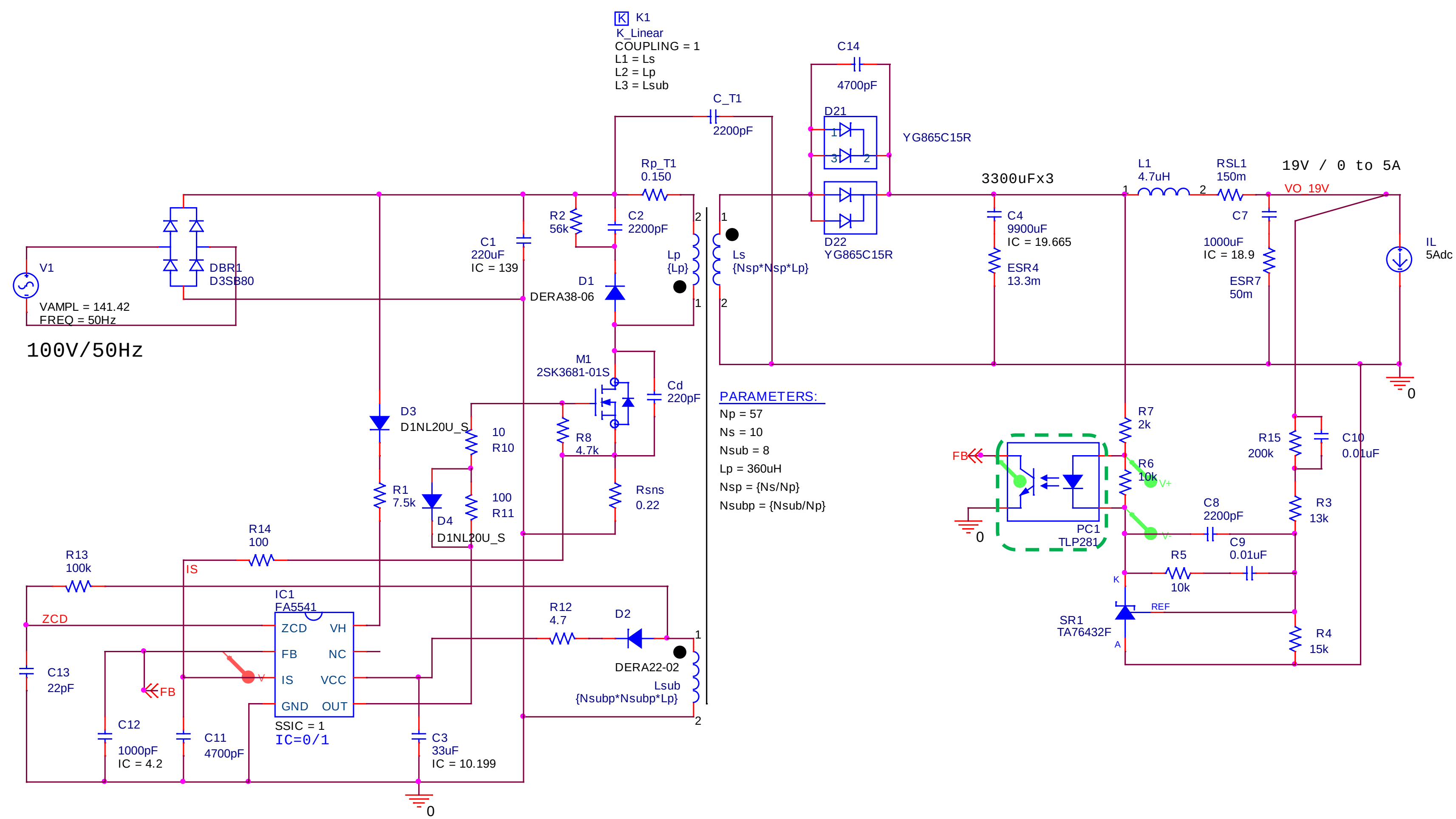
- Simulation results shows the peak value of SBD: V_{KA} and I_F .

9.Schottky barrier diode D21 and D22 waveforms



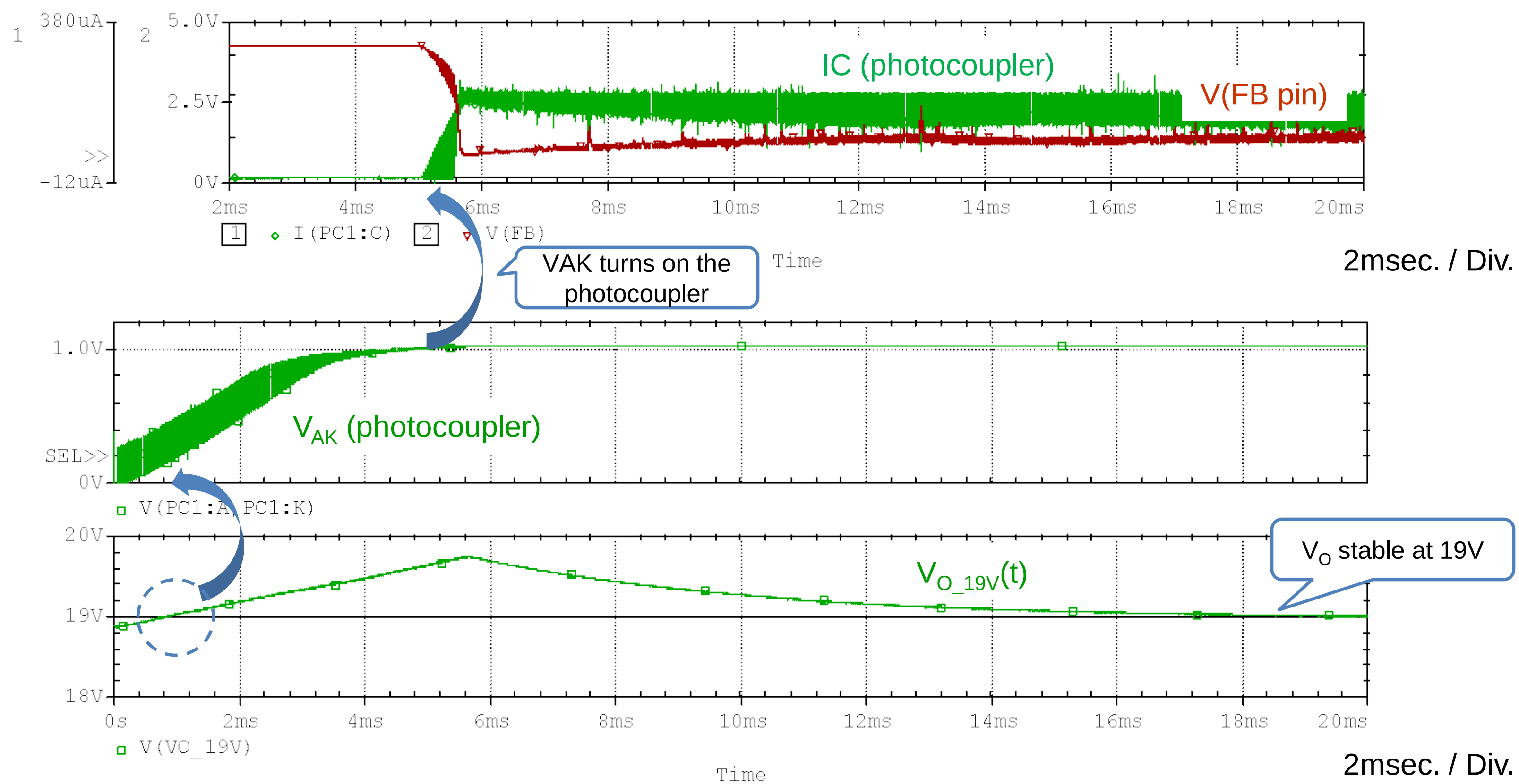
- Simulation results shows the peak value of SBD V_{KA} and I_F . Calculated power loss and average power loss are also shown

10.Photocoupler



※ No parasitic elements: Lleak and ESL ,to aid simulation convergence

10.Photocoupler



- When power supply output reaches spec voltage (19V) ,a shunt regulator draws current through resistor (R6) and VAK of photocoupler increases.
- When VAK turns on photocoupler, collector current Ic increases. This causes FB pin voltage to decreases before power supply output voltage go to the stable state.

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5.	Variable design parameters (Ll_{eak} and C2)	Params