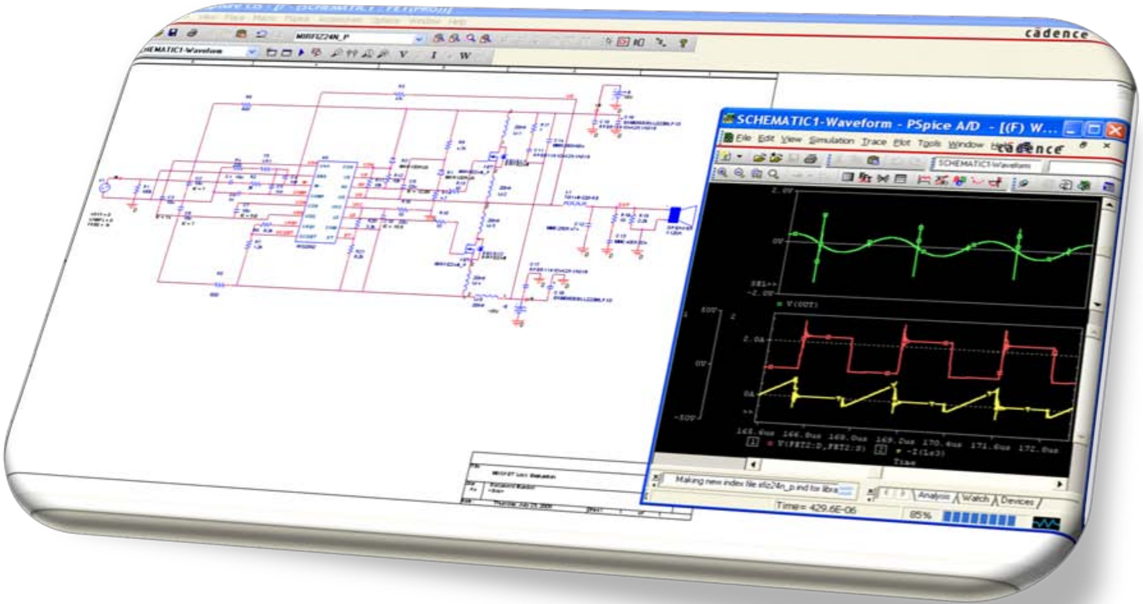
Bee Technologies

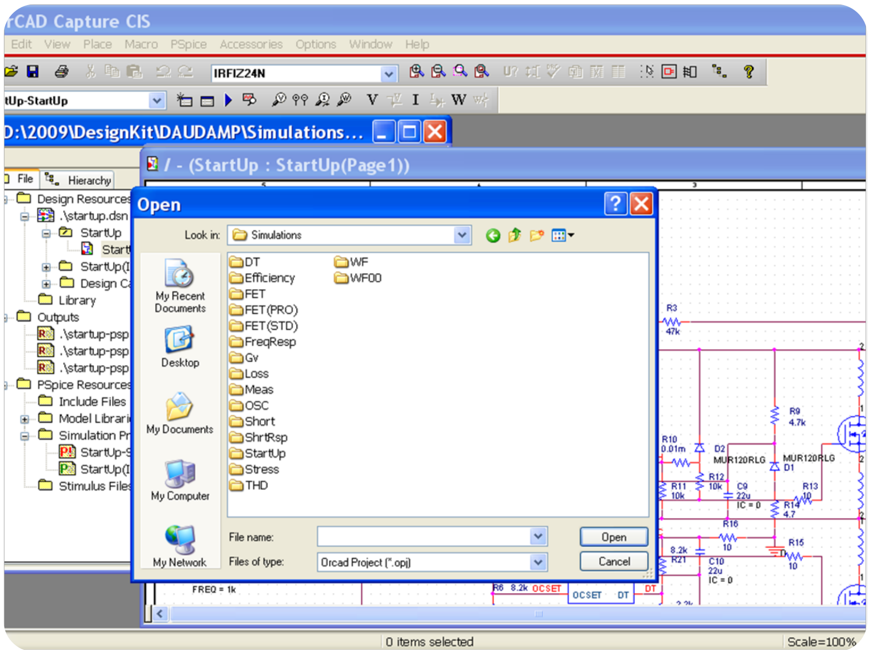


Get Started with DesignKit

Class D Audio Amplifier Using IRS2092

Contents

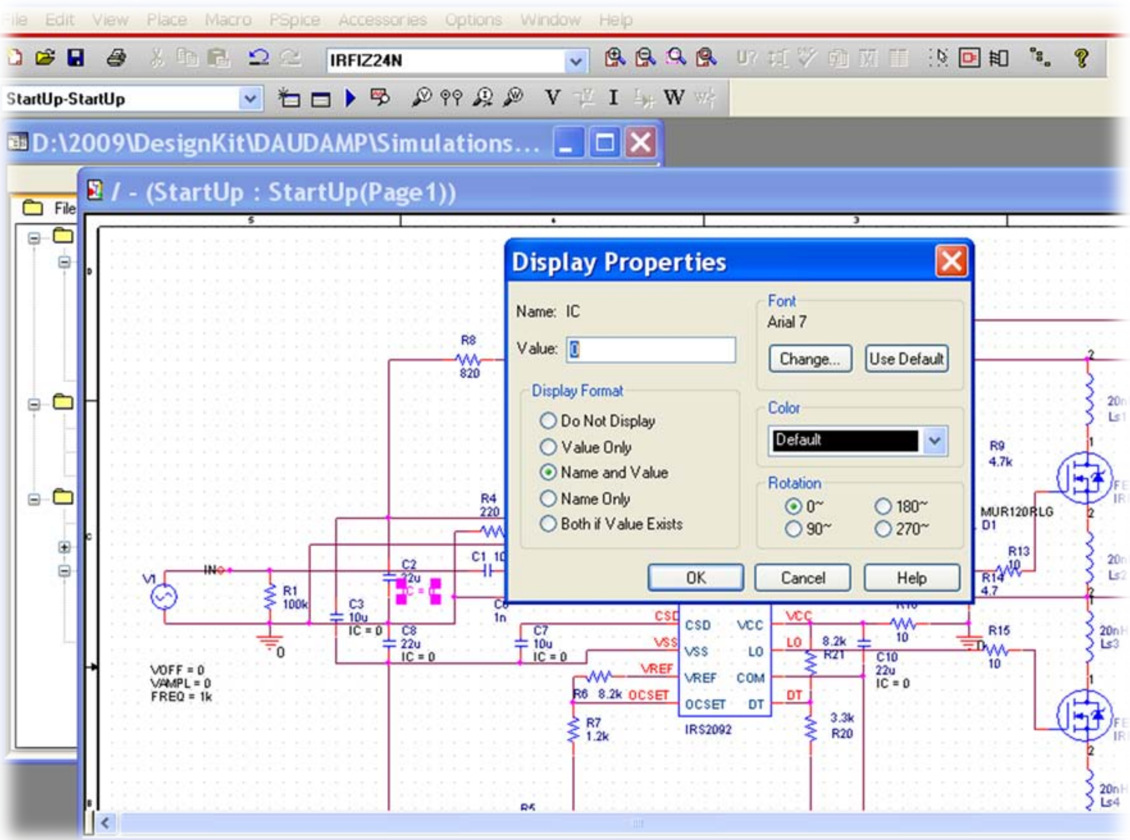
1. DesignKit Simulations folders



- Ready to use simulation projects
  - ✓ Test conditions are set and easily changeable.
  - ✓ Appropriate simulation settings and Initial Condition (.IC).
  - ✓ .Option setting is done without convergence problem.
  - ✓ Libraries are included and added.
  - ✓ Simulation results (ex. Power and %Efficiency) are calculated and displayed.

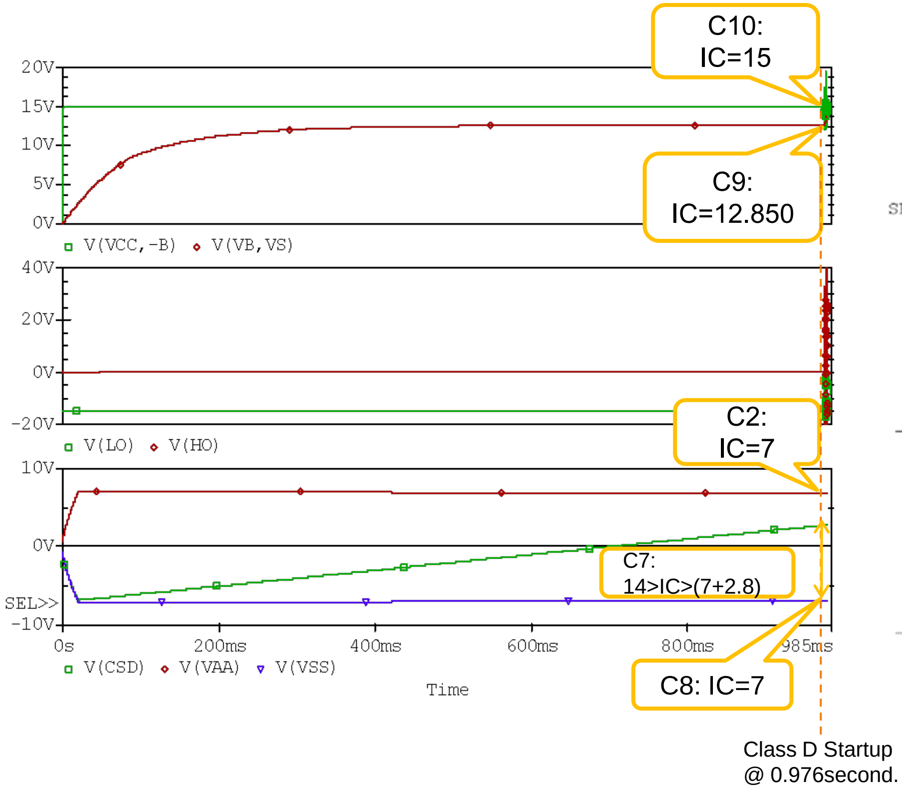
2. How the initial condition are set?

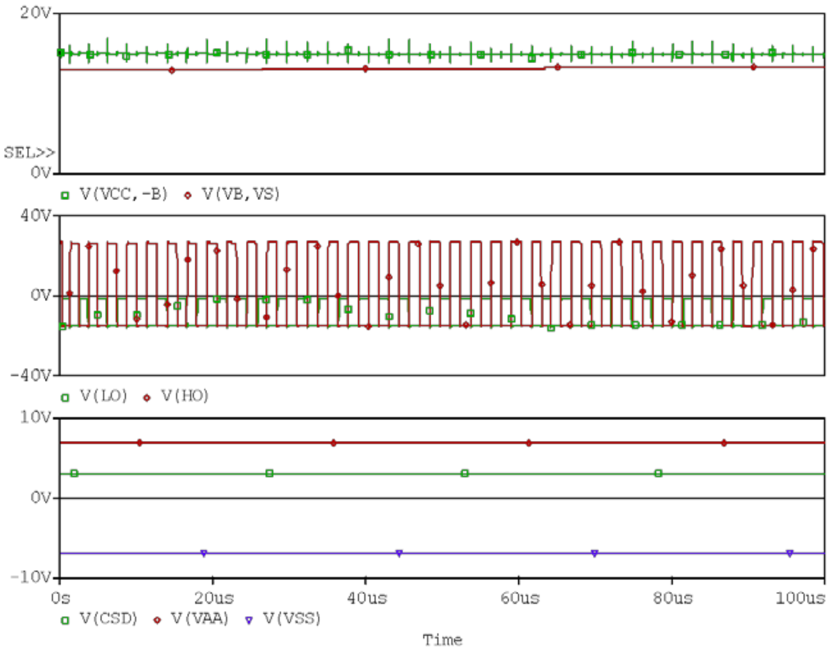
1. Open Project: ...¥Simulations¥StartUp¥StartUp.opj .
2. Set initial value of charged-up capacitors (C2, C3, C7, C8, C9, and C10) to be zero (IC=0).
3. Run the simulation (0-1sec. or until circuit is startup).



2. How the initial condition are set?

4. Initial conditions are the startup voltage at each capacitor.
5. Change the IC values ,then run the simulation (0-100usec. with maximum time step 10nsec.).



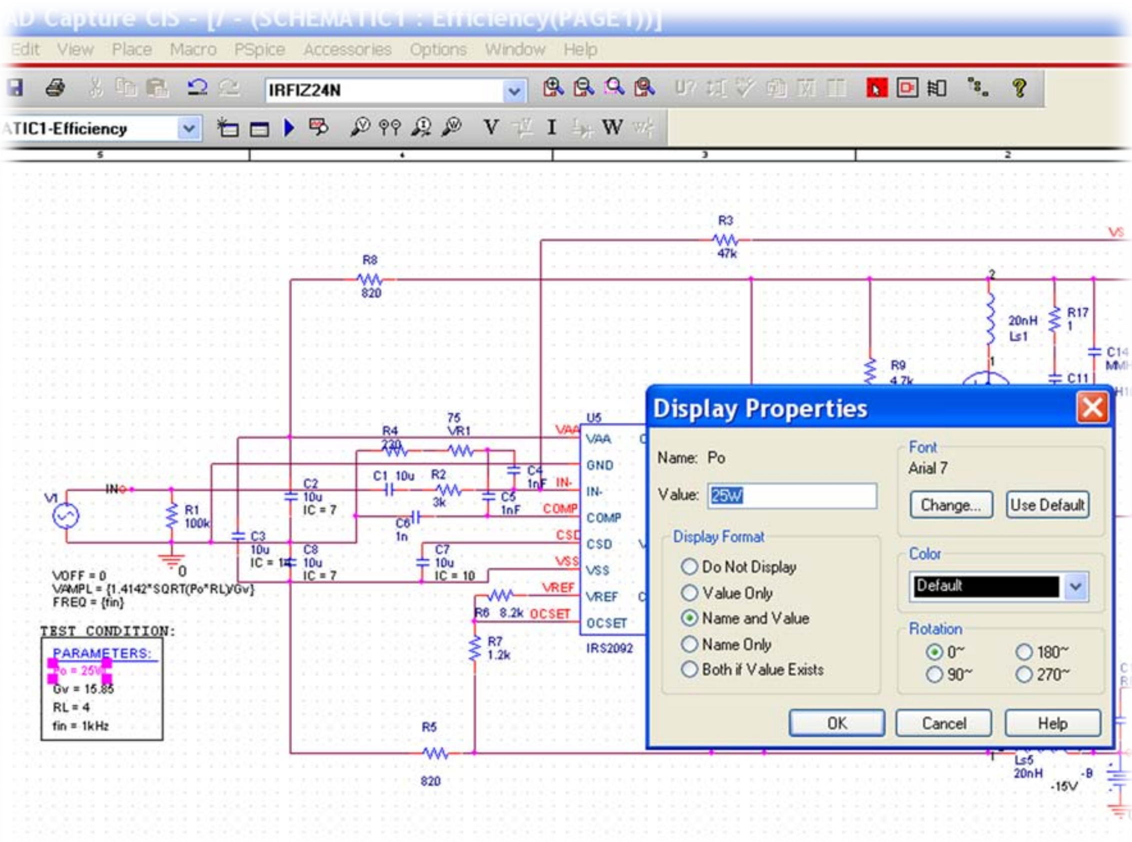


3. Example of Using Design Kit

- Estimate design specification.
  - ✓ %Efficiency.
  - ✓ %THD.
  - ✓ Frequency response.
- Create reference waveforms.
- Change the design parameters and simulate to see results.
- Component stress test.
- Simulate switching losses.
- Simulate Short-circuit scenarios.

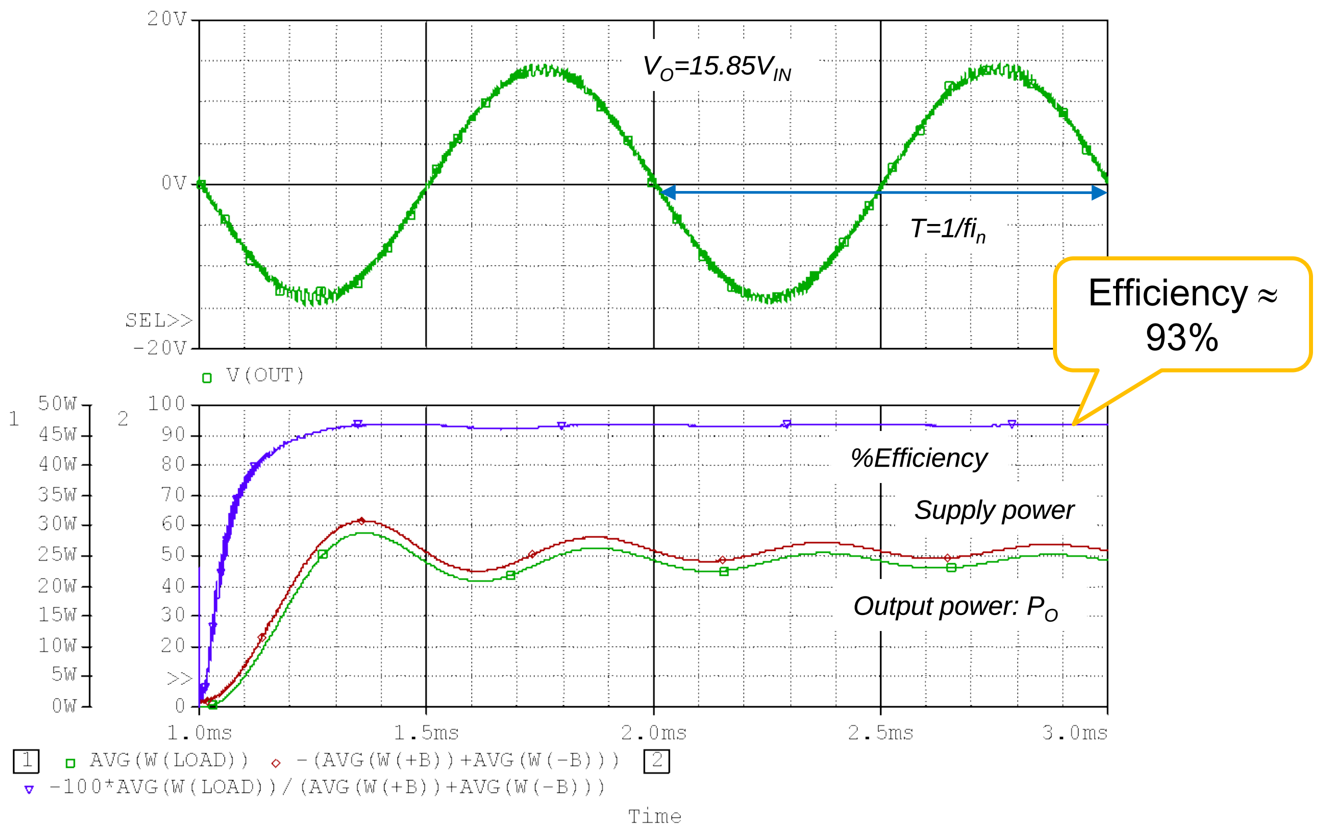
4. How to Estimate Design %Efficiency?

1. Open Project: ...¥Simulations¥**Efficiency¥Efficiency.opj** .
2. Enter test condition parameters: P_O=25W, G_V=15.85(24dB), R_L=4ohm, and f_{in}=1kHz.
3. Run the simulation from 1 to 3 ms. (about 3×1kHz output cycles)



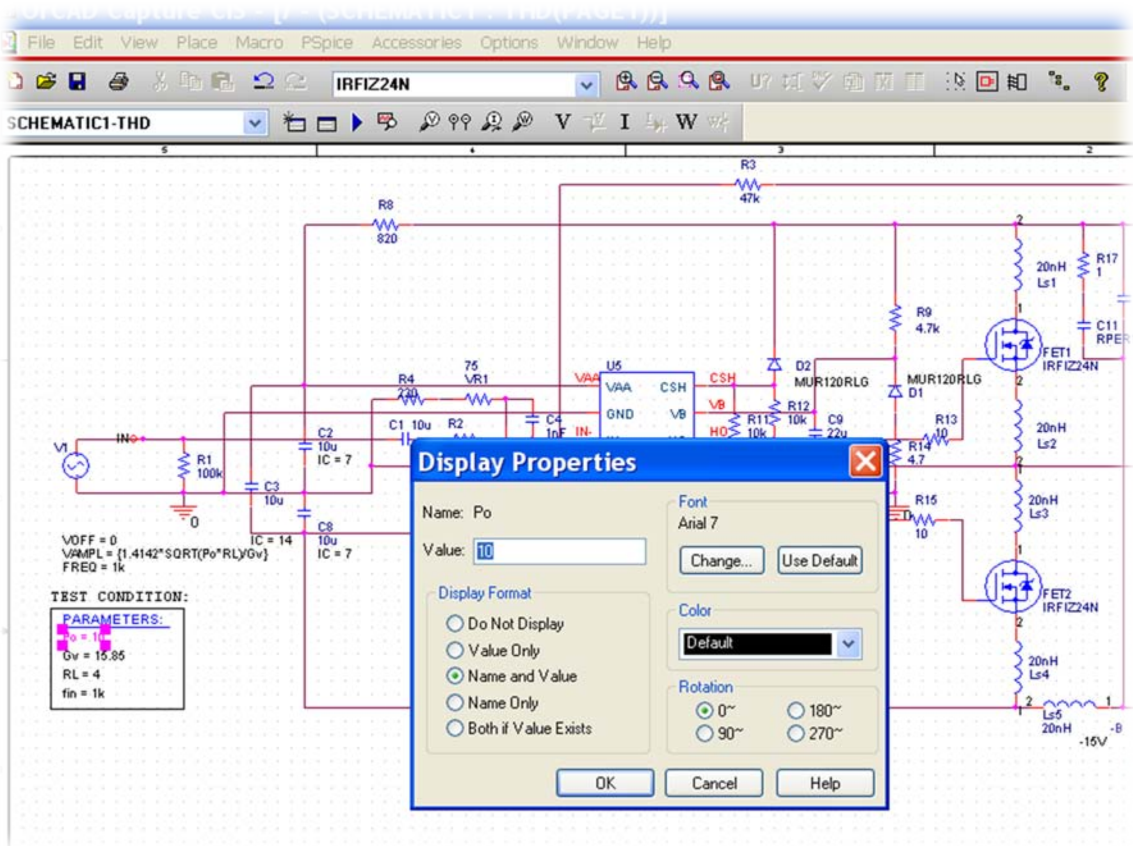
4. How to Estimate Design %Efficiency?

4. Add traces: "AVG(W(LOAD))" for PO[W],
"-(AVG(W(+B))+AVG(W(-B)))" for Supply power [W], and
"-100*AVG(W(LOAD))/(AVG(W(+B))+AVG(W(-B)))" for %Efficiency



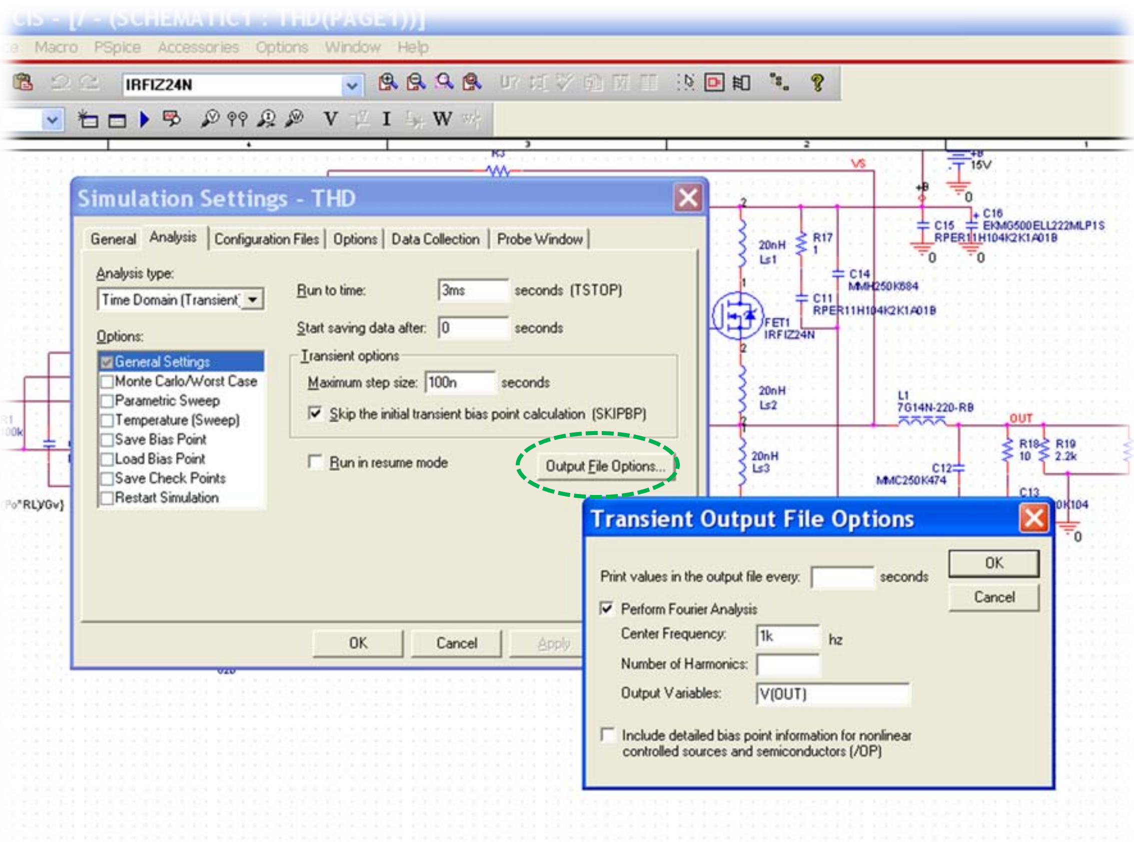
5. How to Estimate Output THD?

1. Open Project: ...¥Simulations¥**THD¥THD.opj** .
2. Enter test condition parameters: P_O=10W, G_V=15.85(24dB), R_L=4ohm, and f_{in}=1kHz.



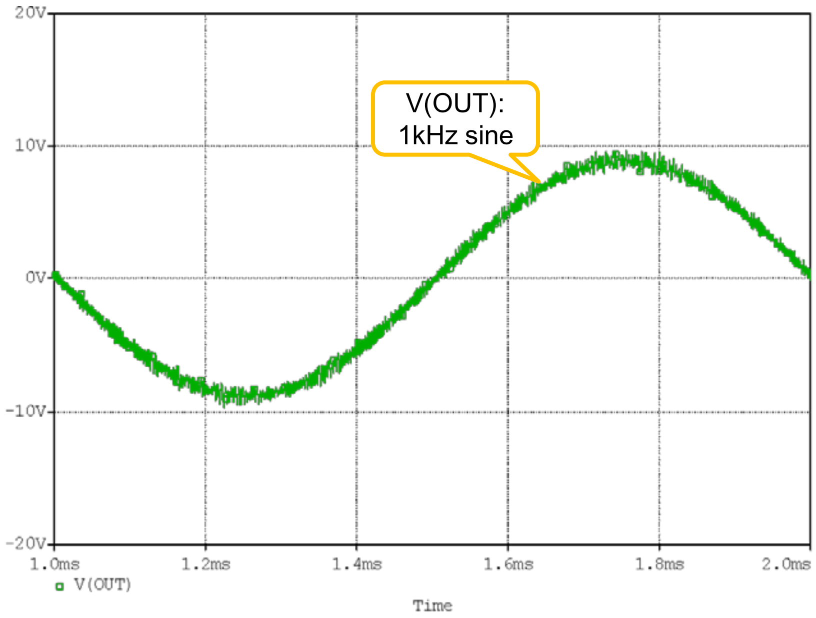
5. How to Estimate Output THD?

3. THD is calculated by checking the box “Perform Fourier Analysis” in the Output File Options setting. Center Frequency is 1kHz same as f_{in} and “V(OUT)” is the Output Variable(s).



5. How to Estimate Output THD?

4. Run the simulation 0 to 3ms. (maximum time step 100ns.).
5. View Output File to see the simulated result THD(%)



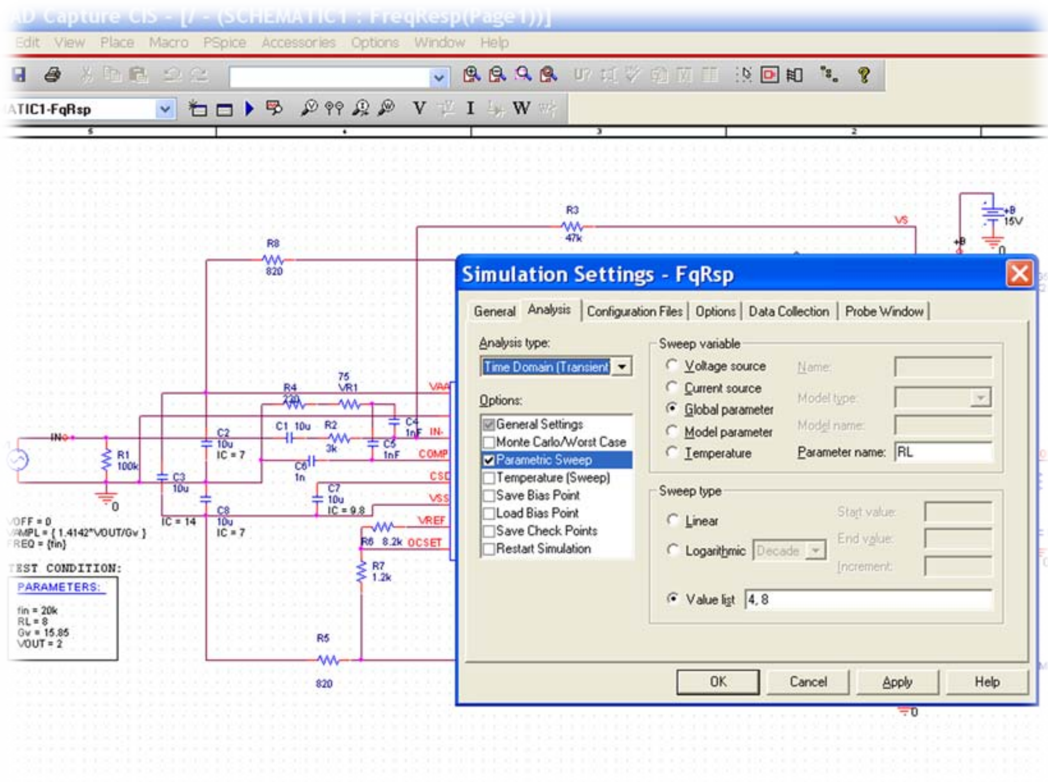
HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE
1	1.00E+03	8.81E+00	1.00E+00	1.79E+02	0.00E+00
2	2.00E+03	4.62E-04	5.25E-05	4.18E+01	-3.15E+02
3	3.00E+03	2.78E-04	3.16E-05	8.49E+01	-4.51E+02
4	4.00E+03	3.23E-04	3.67E-05	6.91E+01	-6.45E+02
5	5.00E+03	3.73E-04	4.23E-05	8.66E+01	-8.06E+02
6	6.00E+03	6.69E-04	7.60E-05	6.10E+01	-1.01E+03
7	7.00E+03	2.85E-04	3.24E-05	8.09E+01	-1.17E+03
8	8.00E+03	4.32E-04	4.91E-05	7.17E+01	-1.36E+03
9	9.00E+03	5.95E-04	6.76E-05	2.70E+01	-1.58E+03

TOTAL HARMONIC DISTORTION = 1.438206E-02 PERCENT

※ Please note that the simulated result is only an estimate of %THD and the value is influenced by maximum step size.

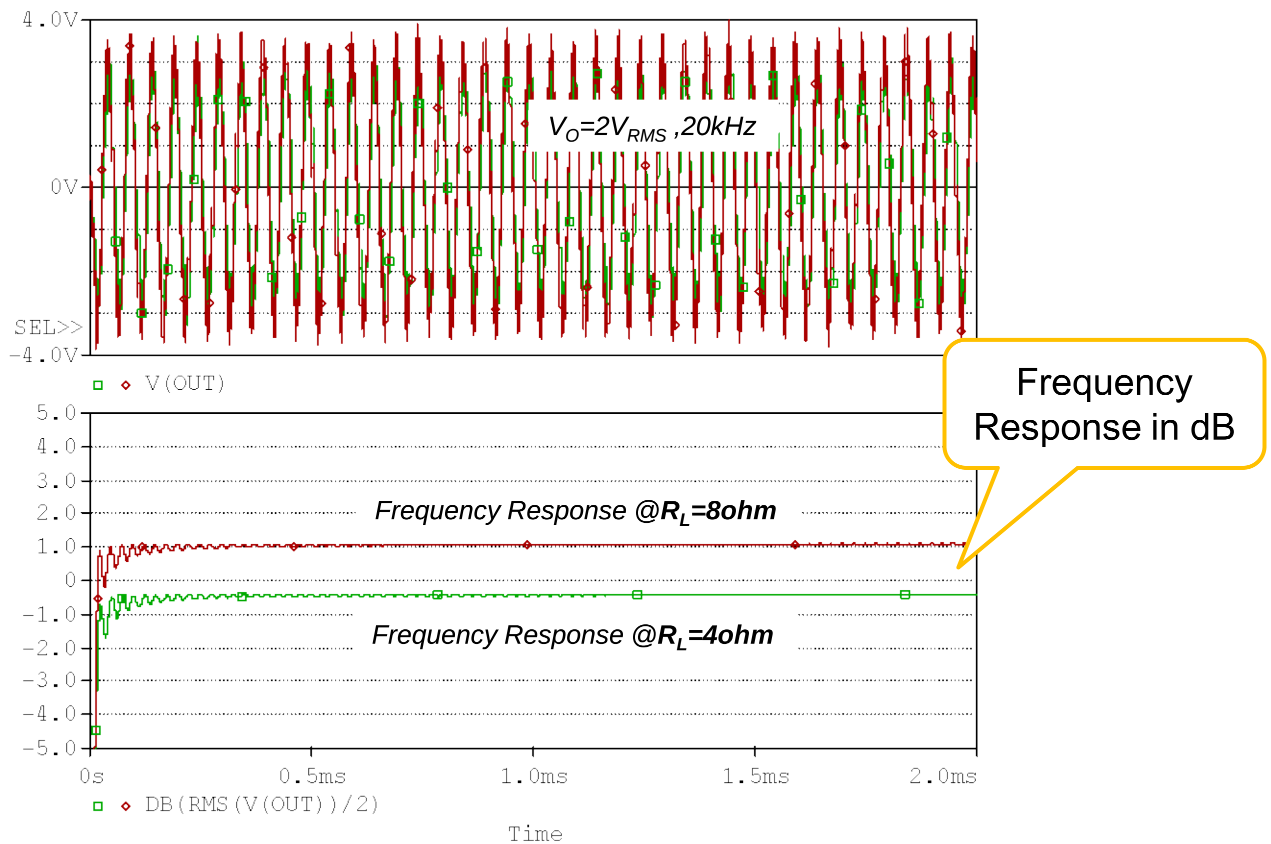
6. How to Estimate Frequency Response?

1. Open Project: ...¥Simulations¥**FrqRsp¥FreqResp.opj**.
2. Enter test condition parameters: V_{OUT}**=2V**, G_V=15.85(24dB), R_L=4/8 ohm, and f_{in}=20kHz.
3. Run the simulation from 0 to 2 ms. (about 40×20kHz output cycles). Use Parametric Sweep (Global parameter: RL with value = 4 and 8)



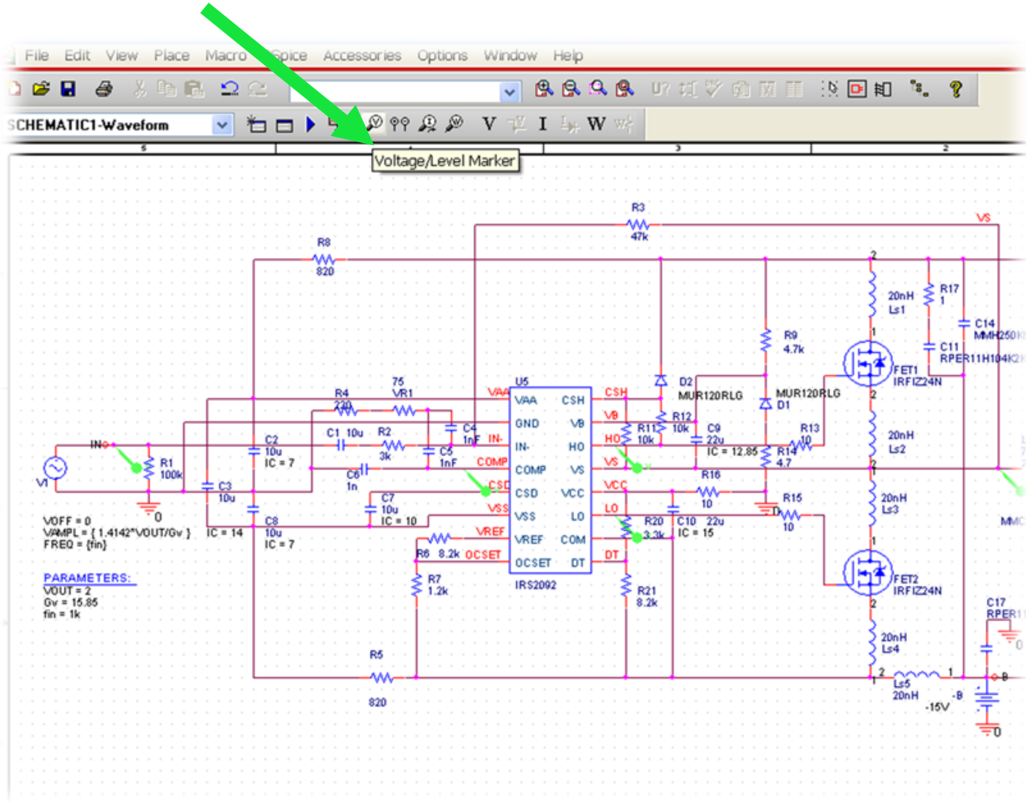
6. How to Estimate Frequency Response?

4. Add traces: " `DB(RMS(V(OUT))/2)`" for the frequency response of $2V_{RMS}$ output in dB.



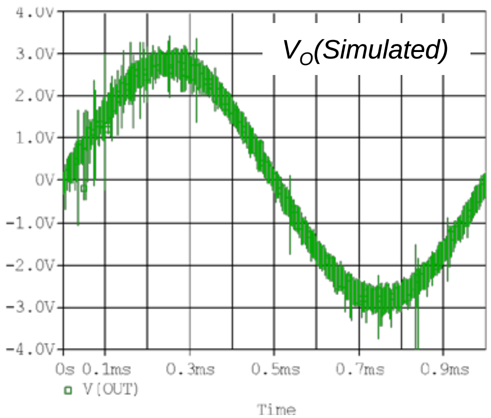
7. How to Create Reference Waveforms?

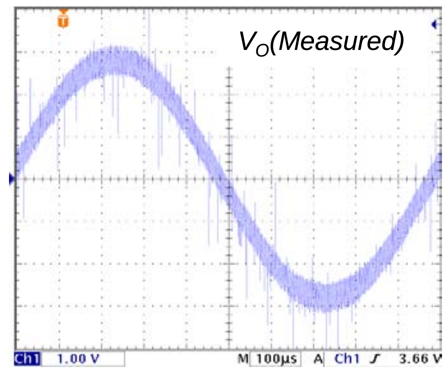
1. Open Project: ...¥Simulations¥**Waveforms¥Waveform.opj** .
2. Enter test condition parameters: V_{OUT}=2V, G_V=15.85(24dB), R_L=4ohm, and f_{in}=1kHz.
3. Run the simulation from 100n to 3 ms. (about 3×1kHz output cycles)
4. Put the Voltage/Level Marker (or Current Marker) to see the waveform(s).



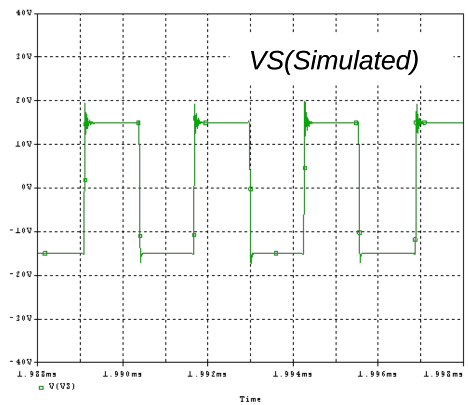
7. How to Create Reference Waveforms?

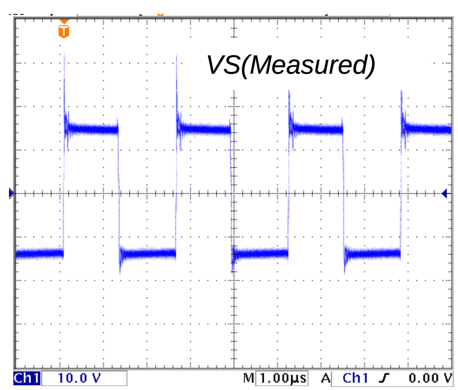
4. Set X and Y Data Range in Axis Setting according to oscilloscope scale.
5. Use simulated waveforms as reference to compare with real circuit waveforms.





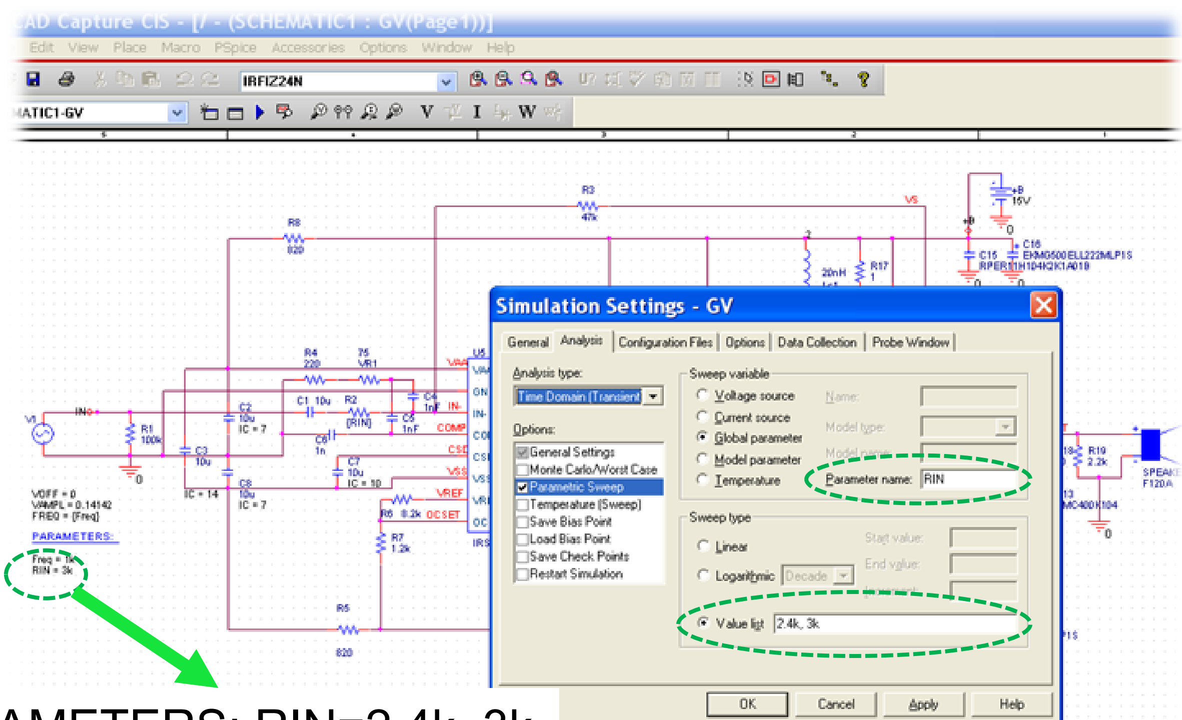
Result are correlated according to simulated data.





8. Change R_{IN} (R2) and simulate to see change in G_V

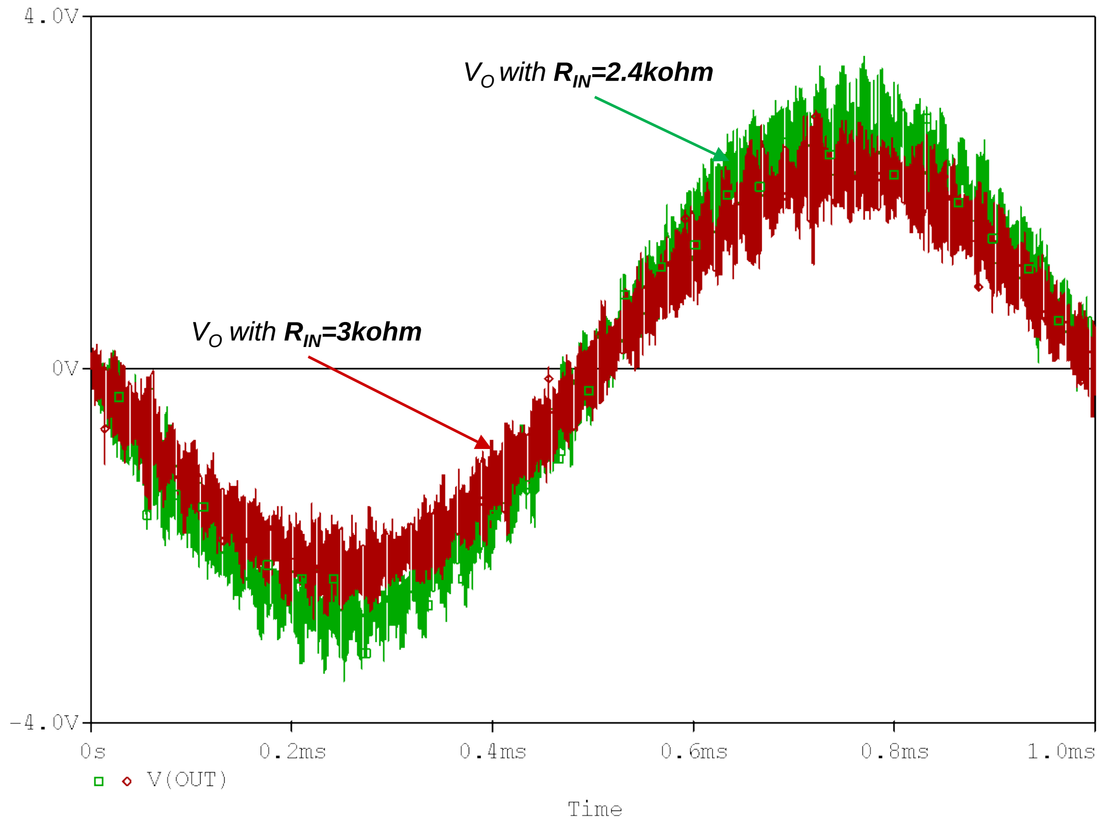
1. Open Project: ...¥Simulations¥**Gv¥Gv.opj**.
2. Enter test condition parameters: V_{IN}=100mV_{RMS}(0.14142V_{PEAK}), **R_{IN}=2.4 / 3 kohm**, R_L=8 ohm (speaker), and f_{in}=1kHz.
3. Run the simulation from 0 to 1 ms. (about 1×1kHz output cycles). Use Parametric Sweep (Global parameter: RIN with value = 2.4k and 3k)



PARAMETERS: RIN=2.4k, 3k

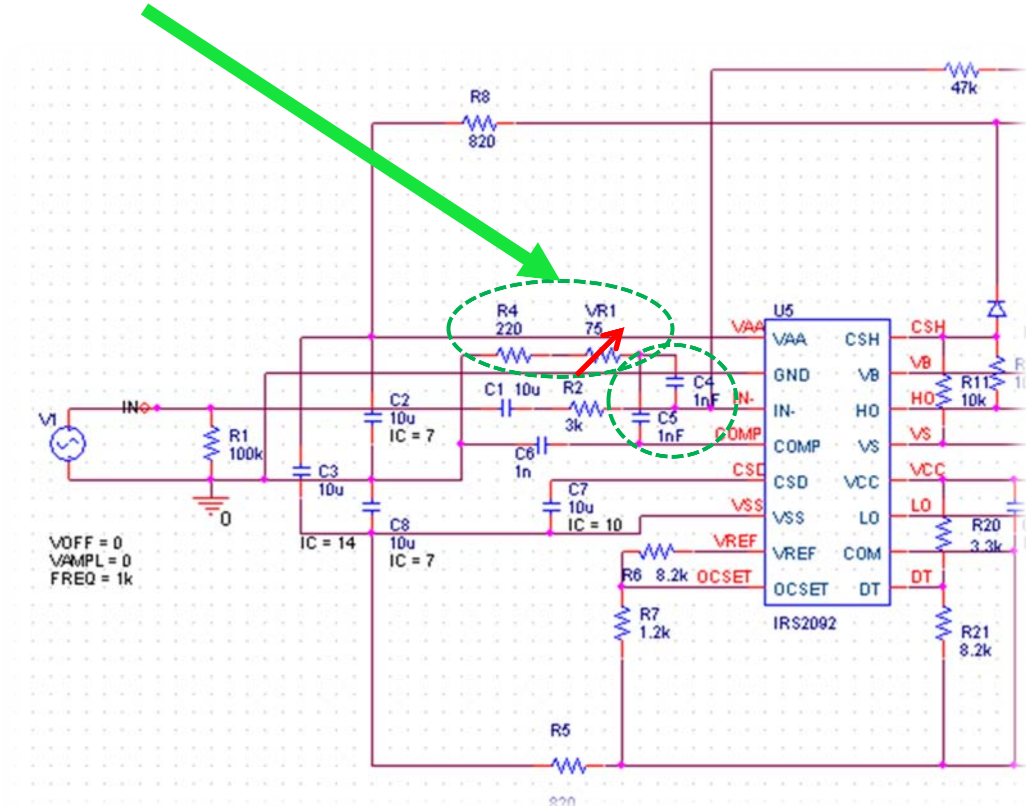
8. Change R_{IN} (R2) and simulate to see change in G_V

4. Simulated result shows Vo with different gain G_V.
5. Change parameter: RIN until you get a satisfied result.



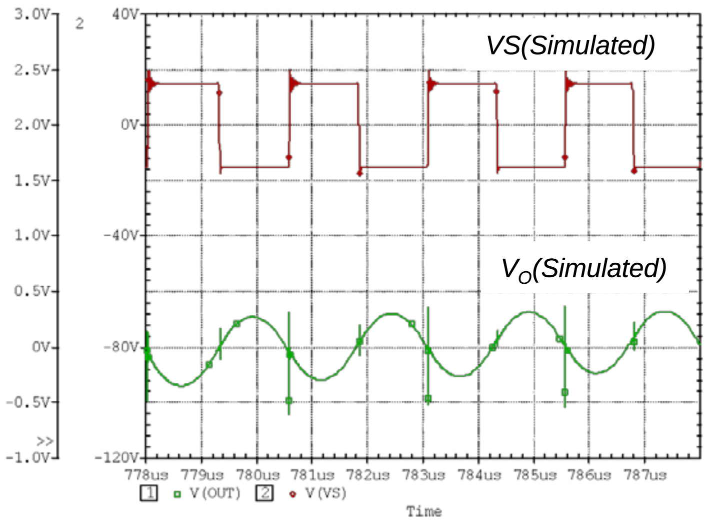
9. Use Design Kit to select proper VR value

1. Open Project: ...¥Simulations¥**OSC¥Waveform.opj**.
2. Input voltage: V_{IN}=0, R_L=8 ohm (speaker).
3. f_{OSC}=400kHz is chosen for this design, C4=C5=1nF, R4=220, a variable resistor: VR1 value will be varied.

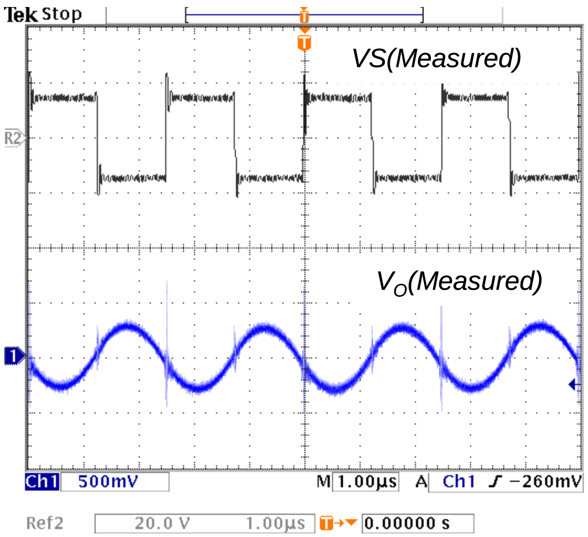


9. Use Design Kit to select proper VR value

4. Change VR1 value until simulation result with f_{OSC}=400kHz (VR1=75ohm).
5. Choose VR1 that value more than 100 ohm for the design (this time VR1:1k is chosen).



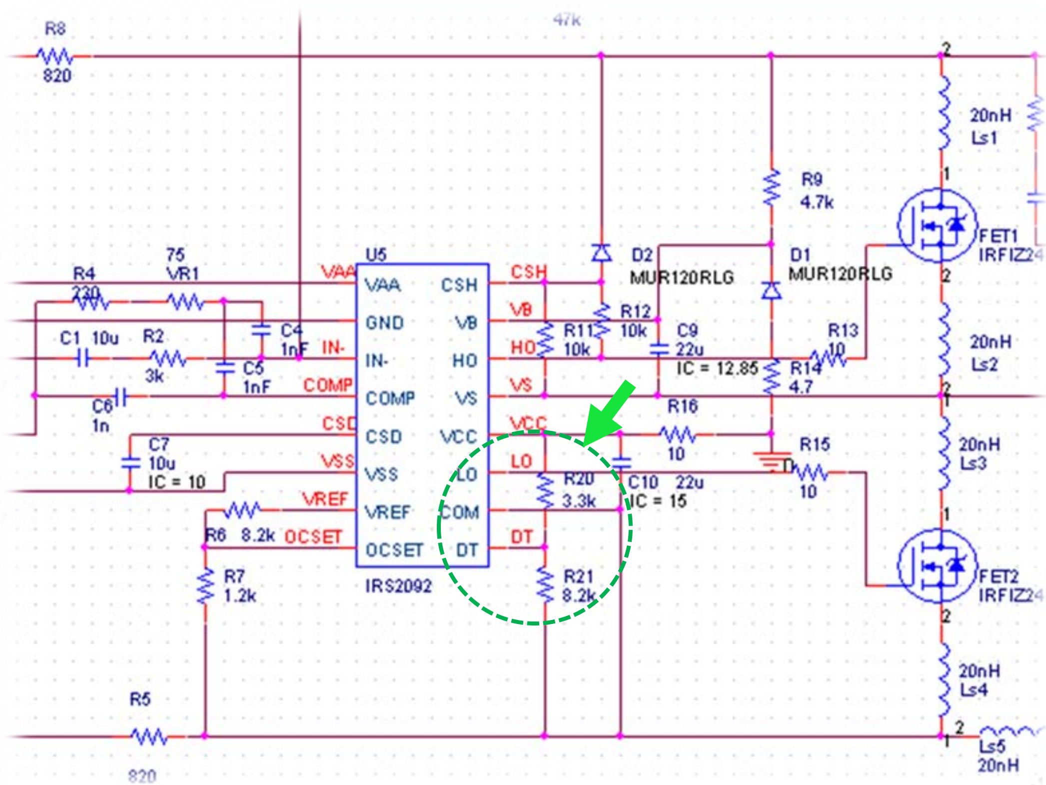
Simulated waveform with VR1: Value=75



Measured waveform from real circuit using VR1: 1k

10. Use Design Kit to Predict Spike Voltage vs. Dead-time setting

1. Open Project: ...¥Simulations¥**DT¥Waveform.opj**.
2. Input voltage: V_{IN}=0, R_L=8 ohm (speaker).
3. Select dead-time setting DT1: R_{20}=3.3k / R_{21}=8.2k, Simulate and compare result with dead-time setting DT3: R_{20}=8.2k / R_{21}=3.3k

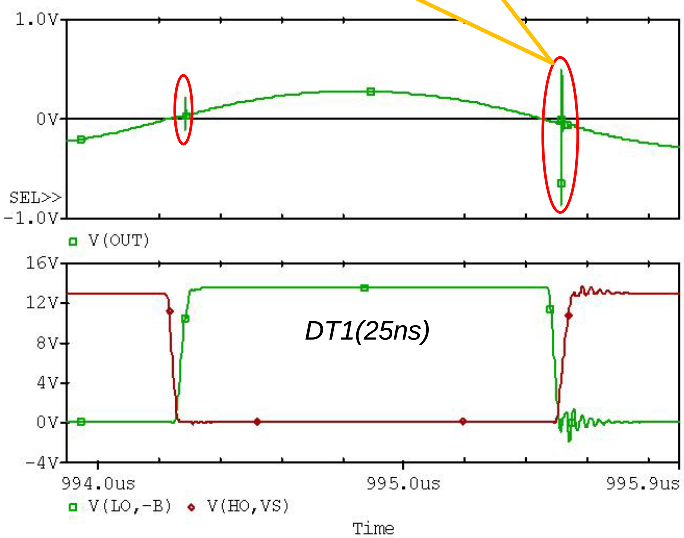


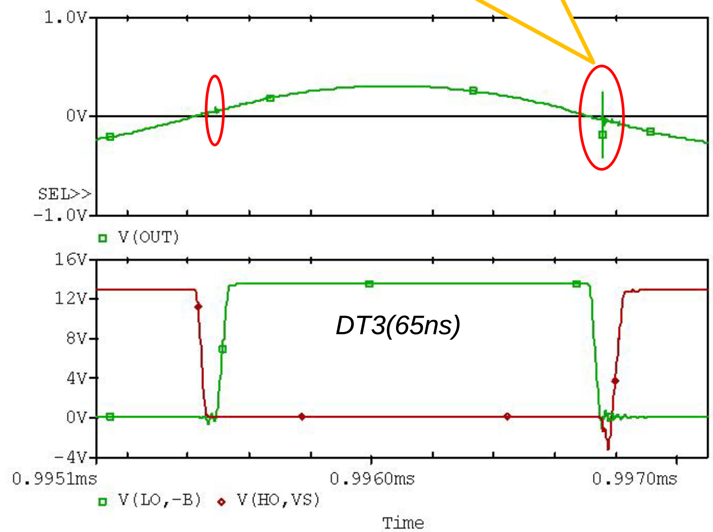
10. Use Design Kit to Predict Spike Voltage vs. Dead-time setting

4. Compare the results to see that spike voltages are acceptable or not for each dead-time setting.

Does spike voltage acceptable?

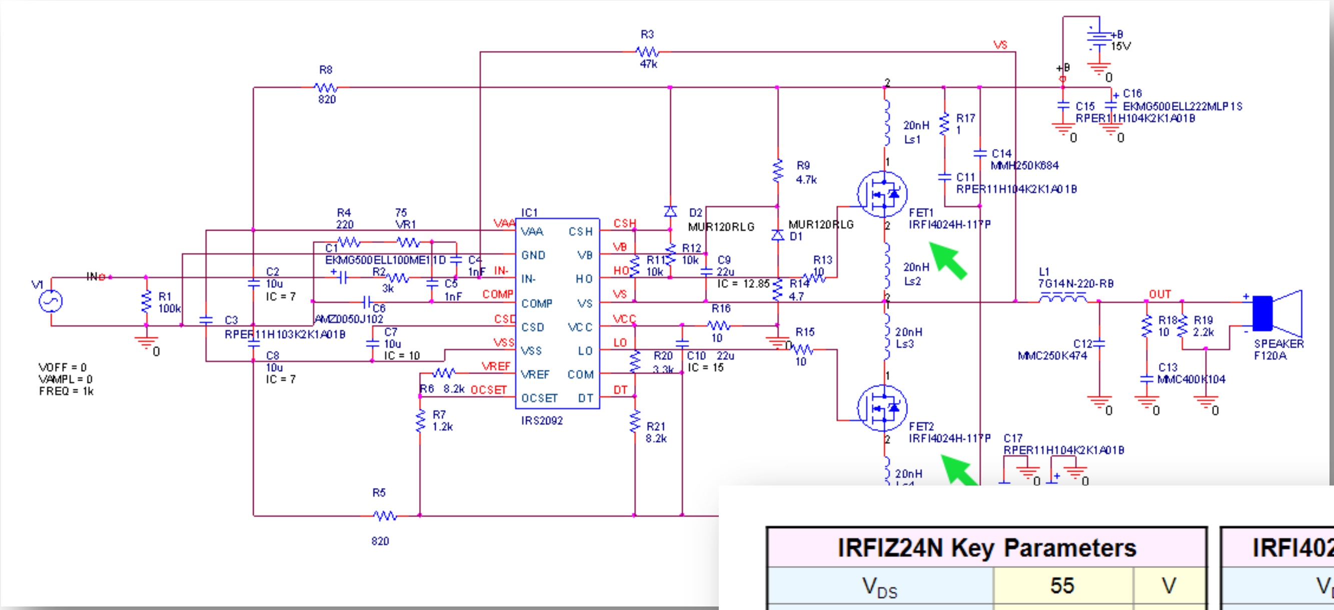
Spike voltage decrease with wider dead-time setting.





11. Use Design Kit to Develop the Design (Change the FETs)

1. Use the simulation files for the performance evaluation (ex. Efficiency, THD, and Waveform).
2. Replace MOSFET model IRFIZ24N with IRFI4024H-117P.
3. Run simulation file to check the design performance.

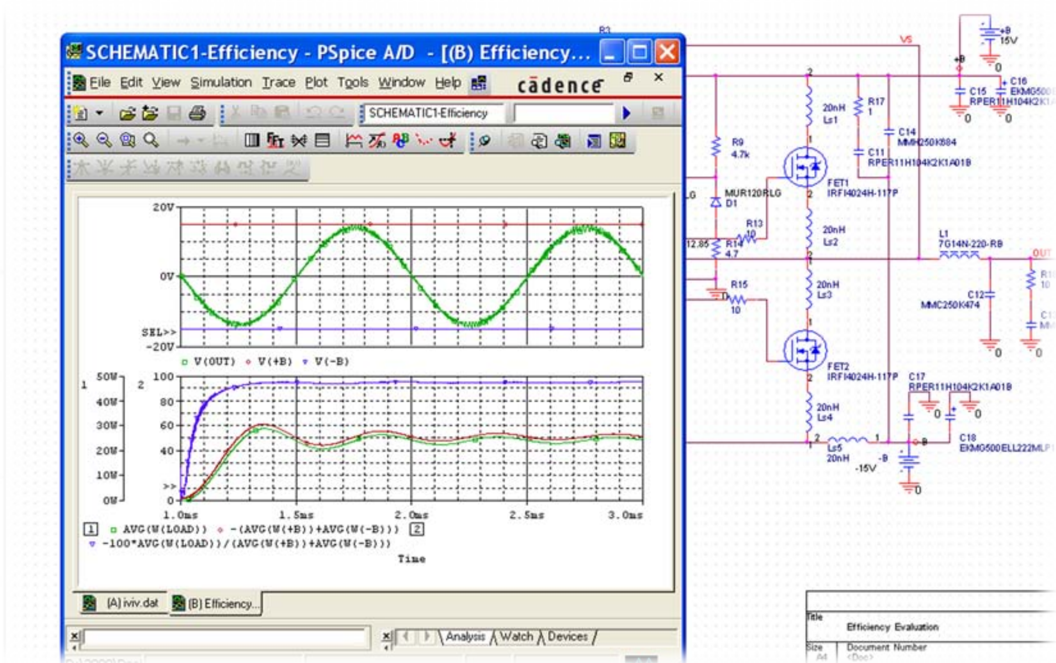


IRFIZ24N Key Parameters		
V_{DS}	55	V
I_D	14	A
$R_{DS(ON)}$ typ. @ 10V	70	mΩ
Q_g typ.	13.4	nC
t_{ON} typ.	38.9	ns
t_{OFF} typ.	46	ns
Q_{rr} typ.	120	nC

IRFI4024H-117P Key Parameters		
V_{DS}	55	V
I_D	11	A
$R_{DS(ON)}$ typ. @ 10V	48	mΩ
Q_g typ.	8.9	nC
t_{ON} typ.	7.9	ns
t_{OFF} typ.	16.4	ns
Q_{rr} typ.	11	nC

11. Use Design Kit to Develop the Design (Change the FETs)

3. Compare the performance of the circuit with difference FET.

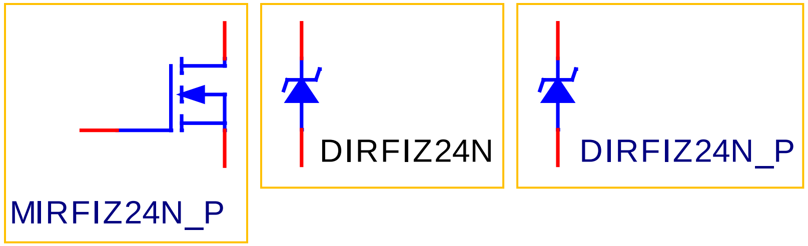


%Efficiency is improved

	IRFIZ24N	IRFI4024H-117P
Efficiency (@ 25W, 4Ω)	93.505%	94.578%
Distortion (@ 1kHz, 4Ω, 10W)	0.0144 %THD	0.0201 %THD

12. MOSFET Professional Model

- Library and symbol files are in folder ...¥Parts¥IRFIZ24N¥IRFIZ24N(PRO)
- IRFIZ24N Professional Model consists of MOSFET Professional (MIRFIZ24N_P), body diode DIRFIZ24N, and body diode Professional DIRFIZ24N_P.
- Use MOSFET Professional model to improve an accuracy Gate Charge characteristics Q_g of FET model.
- Use body diode Professional model to improve an accuracy Reverse Recovery Time characteristic T_{RR} of FET's body diode model.



※ Using Professional model will slow down the simulation time and might cause some convergence error.