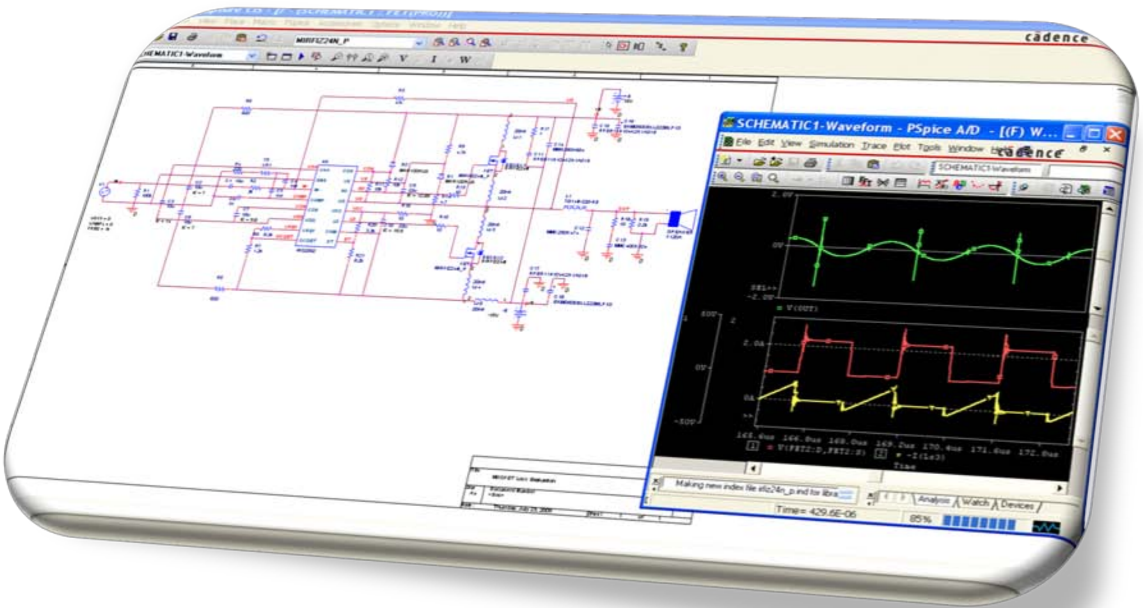

Design Kit

Class D Audio Amplifier Using IRS2092

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Contents

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1. Specifications

General Test Conditions			**Simulation folder**
Supply Voltage	± 15V		
Load Impedance	8-4 Ω		
Self-Oscillating Frequency	400kHz		
Gain Setting	24dB		
Electrical Data			
Output Power	25W	(1kHz, 4Ω)	
Efficiency	93%	(25W, 4Ω)	[Efficiency]
Audio Performance			
Distortion	Less than 0.015%THD	(1kHz, 4Ω, 10W)	[THD]
Frequency Response : 20Hz~20kHz	± 1dB	(20 ~ 20000 Hz, 4Ω, 2V Output)	[FrqRsp]

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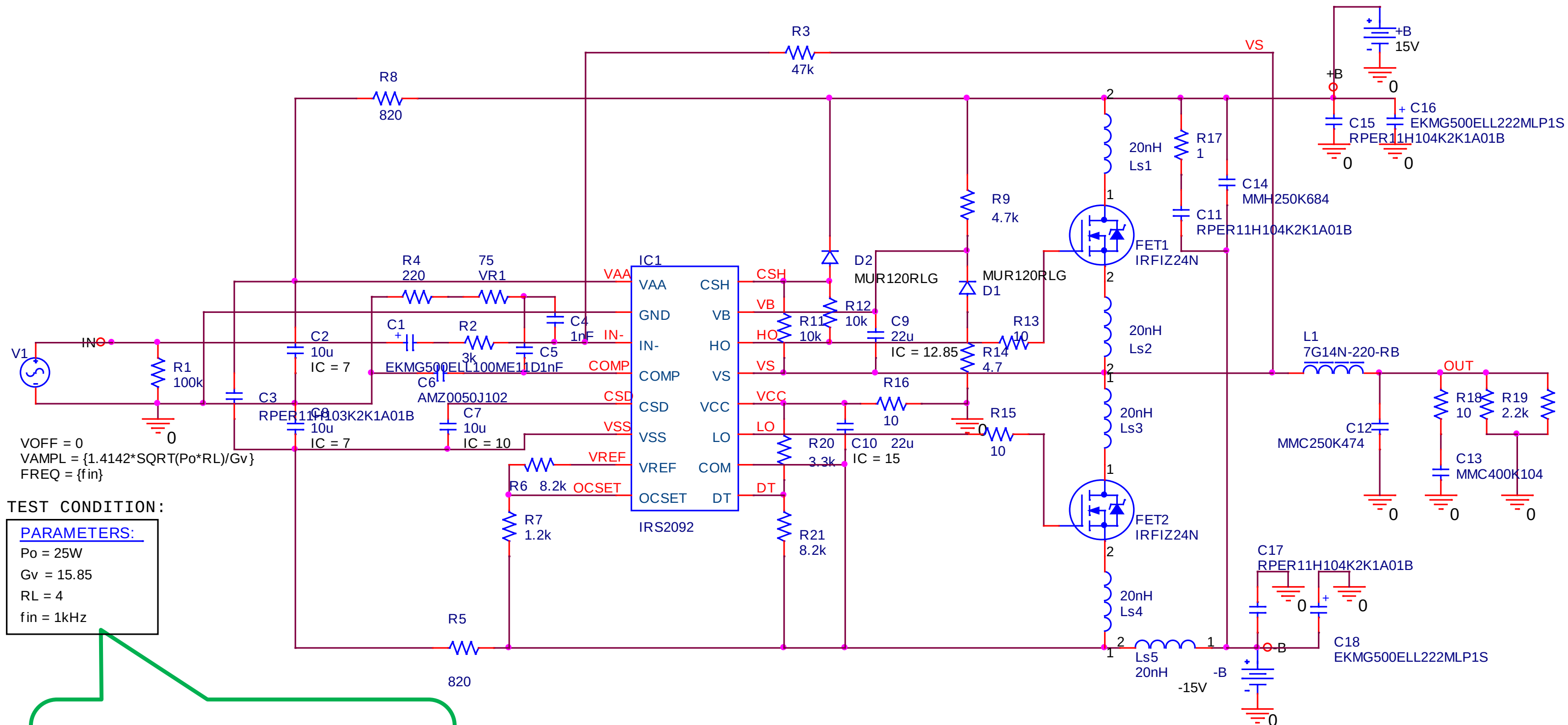
Specifications : Efficiency Evaluation Circuit



Condition :
Po = 25[W], 4Ω Load

Analysis
Time Domain (Transient)
Run to time: 3ms
Start saving data after: 1ms
Maximum step size: 100n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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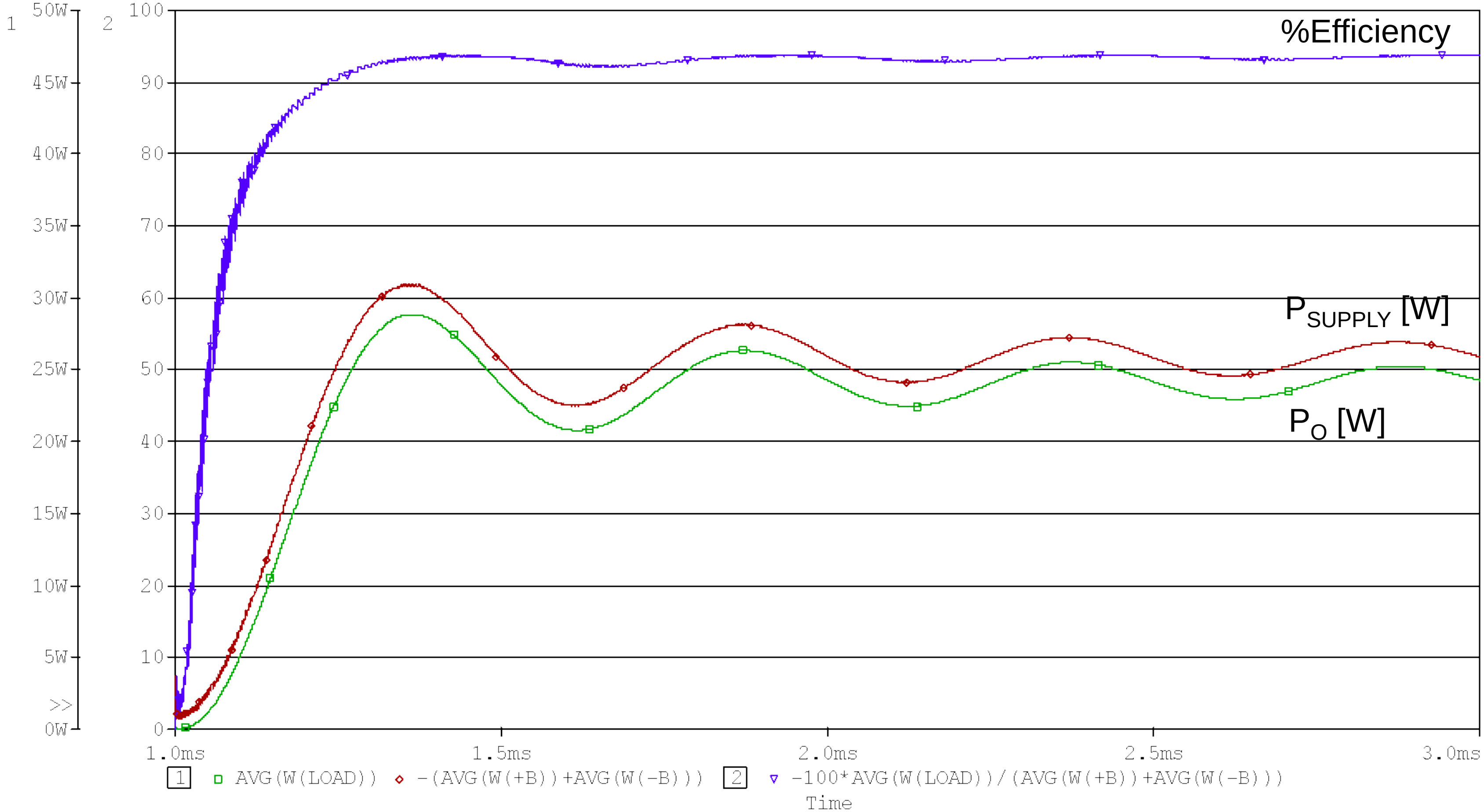
Specifications : Efficiency Simulation Result



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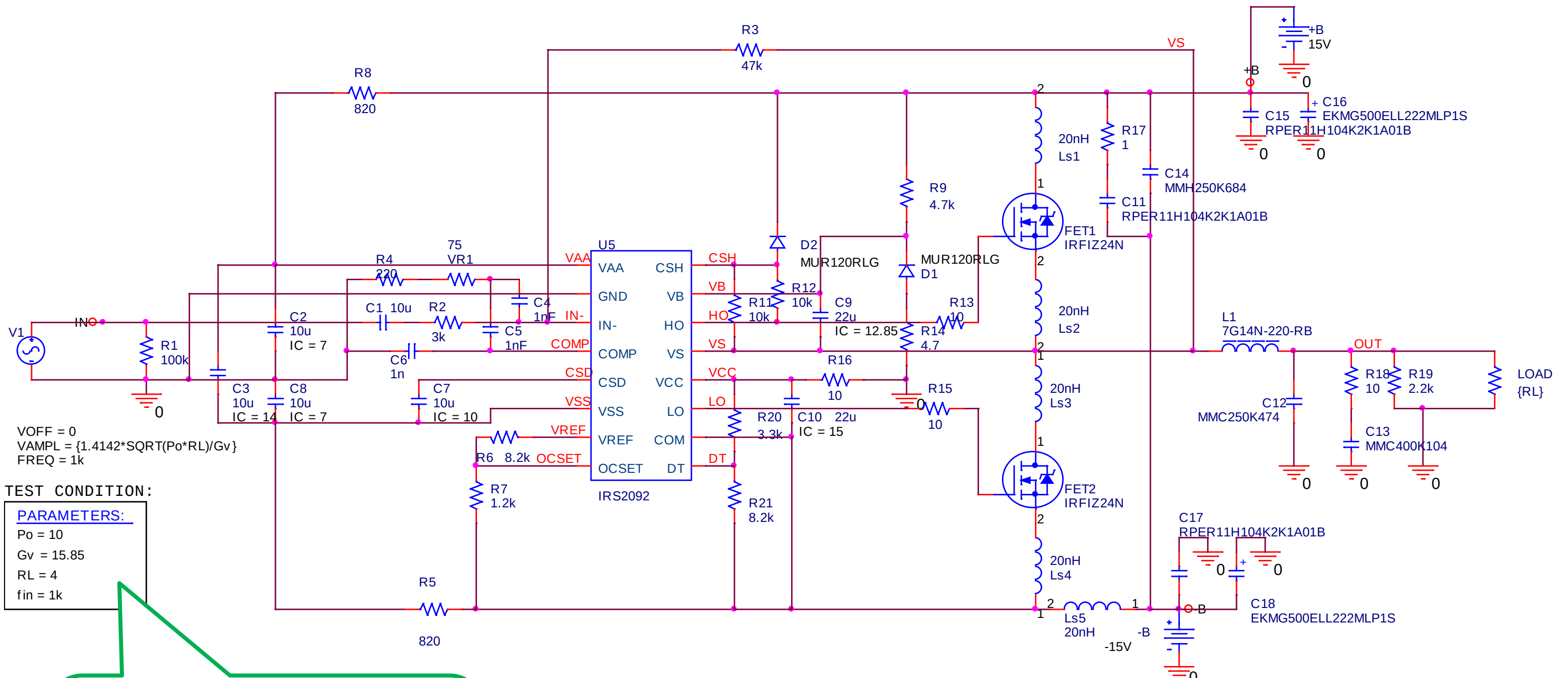
Specifications : THD Evaluation Circuit



Condition :
f_{in} = 1kHz, Po = 10[W],
4Ω Load

Analysis
Time Domain (Transient)
Run to time: 3ms
Start saving data after: 0s
Maximum step size: 100n
☑ Skip the initial transient bias point calculation (SKIPBP)

Output File Options...
☑ Perform Fourier Analysis
Center Frequency: 1khz
Output Variables: V(OUT)

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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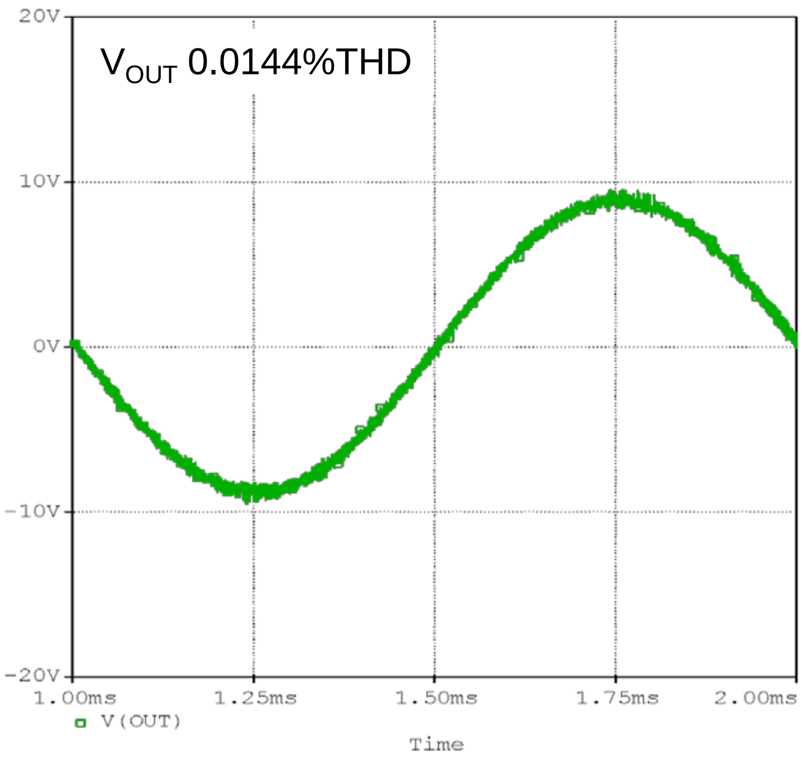
Specifications : THD Simulation Result



HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE
1	1.00E+03	8.81E+00	1.00E+00	1.79E+02	0.00E+00
2	2.00E+03	4.62E-04	5.25E-05	4.18E+01	-3.15E+02
3	3.00E+03	2.78E-04	3.16E-05	8.49E+01	-4.51E+02
4	4.00E+03	3.23E-04	3.67E-05	6.91E+01	-6.45E+02
5	5.00E+03	3.73E-04	4.23E-05	8.66E+01	-8.06E+02
6	6.00E+03	6.69E-04	7.60E-05	6.10E+01	-1.01E+03
7	7.00E+03	2.85E-04	3.24E-05	8.09E+01	-1.17E+03
8	8.00E+03	4.32E-04	4.91E-05	7.17E+01	-1.36E+03
9	9.00E+03	5.95E-04	6.76E-05	2.70E+01	-1.58E+03

TOTAL HARMONIC DISTORTION = 1.438206E-02 PERCENT

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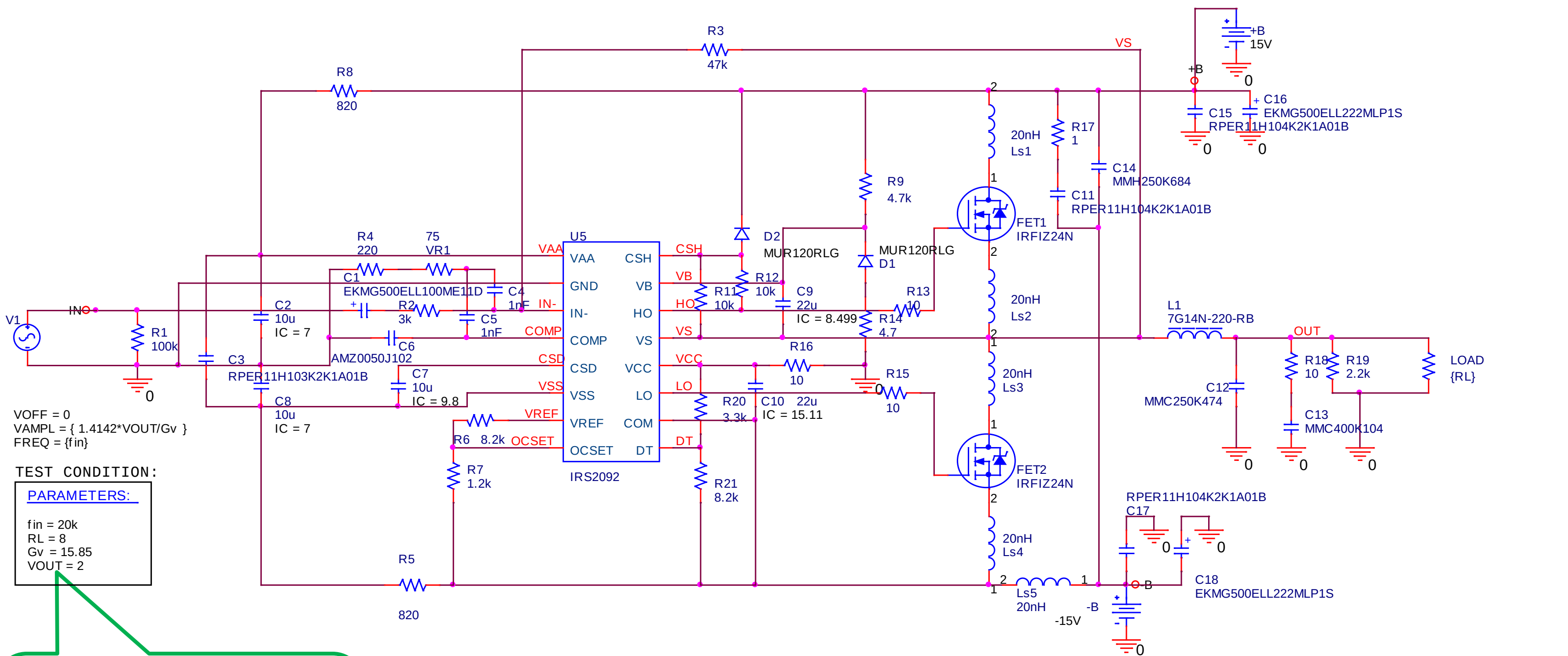
Specifications : Frequency Response Evaluation Circuit



Condition :
20 ~ 20000 Hz, 4Ω
Load, 2V Output

Analysis
Time Domain (Transient)
- Run to time: 2ms
- Start saving data after: 0ms
- Maximum step size: 100n
- ☑ Skip the initial transient bias point calculation (SKIPBP)

Parametric Sweep
- ⦿ Global parameter
  - Parameter name: RL
  - ⦿ Value list: 4, 8

.Options
- RELTOL: 0.01
- VNTOL: 1.0u
- ABSTOL: 1.0n
- CHGTOL: 0.01p
- GMIN: 1.0E-12
- ITL1: 500
- ITL2: 200
- ITL4: 10

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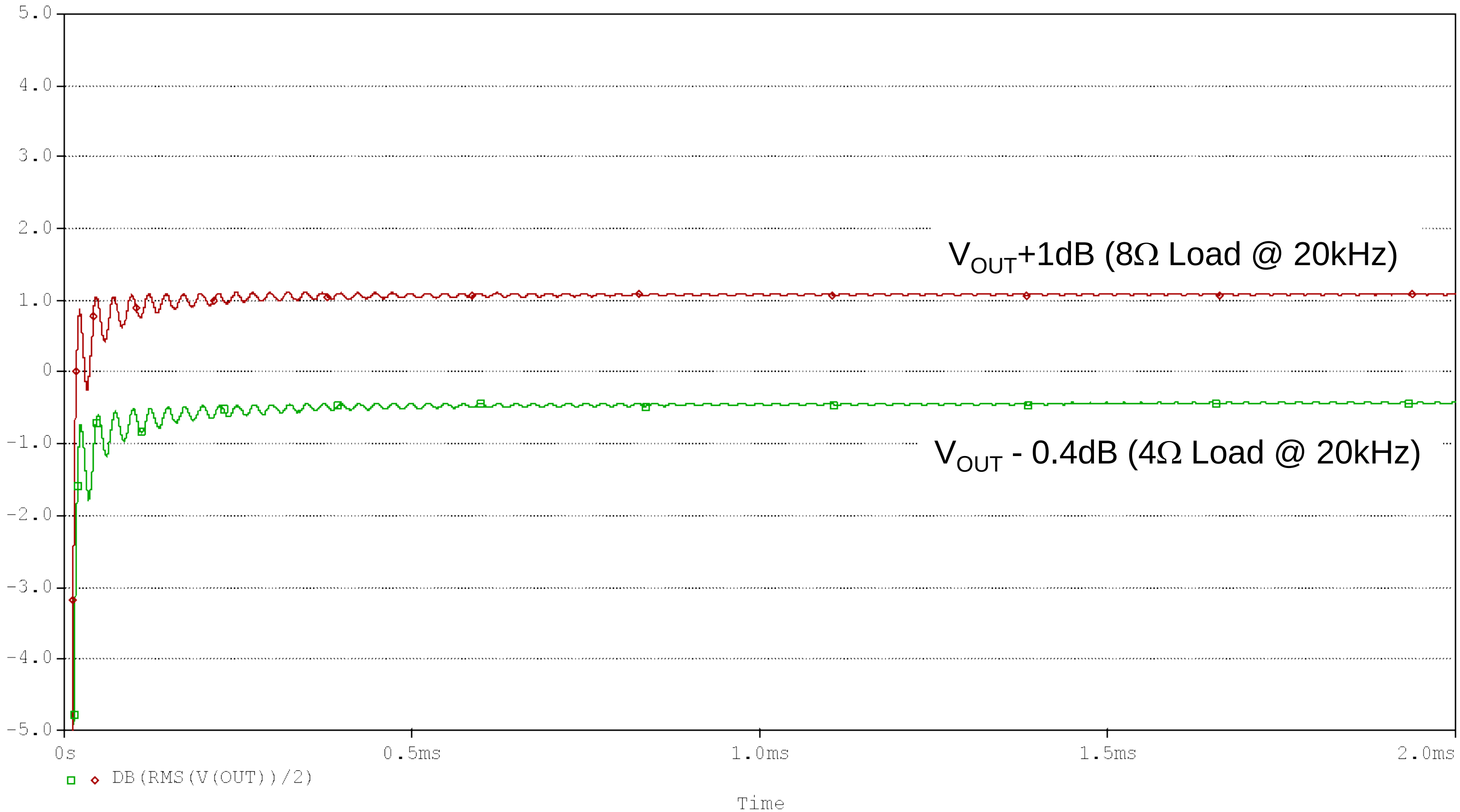
Specifications : Frequency Response Simulation Result



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Note : P_O [W] vs. V_{IN} [V_{PEAK}]

$$Vin\ [Vpeak] = \frac{1.4142 \times \sqrt{Po \times Rload}}{Gv}$$

- Po [W] = power output
- Rload [Ω] = Load resistance
- G_V = Amplifier voltage gain

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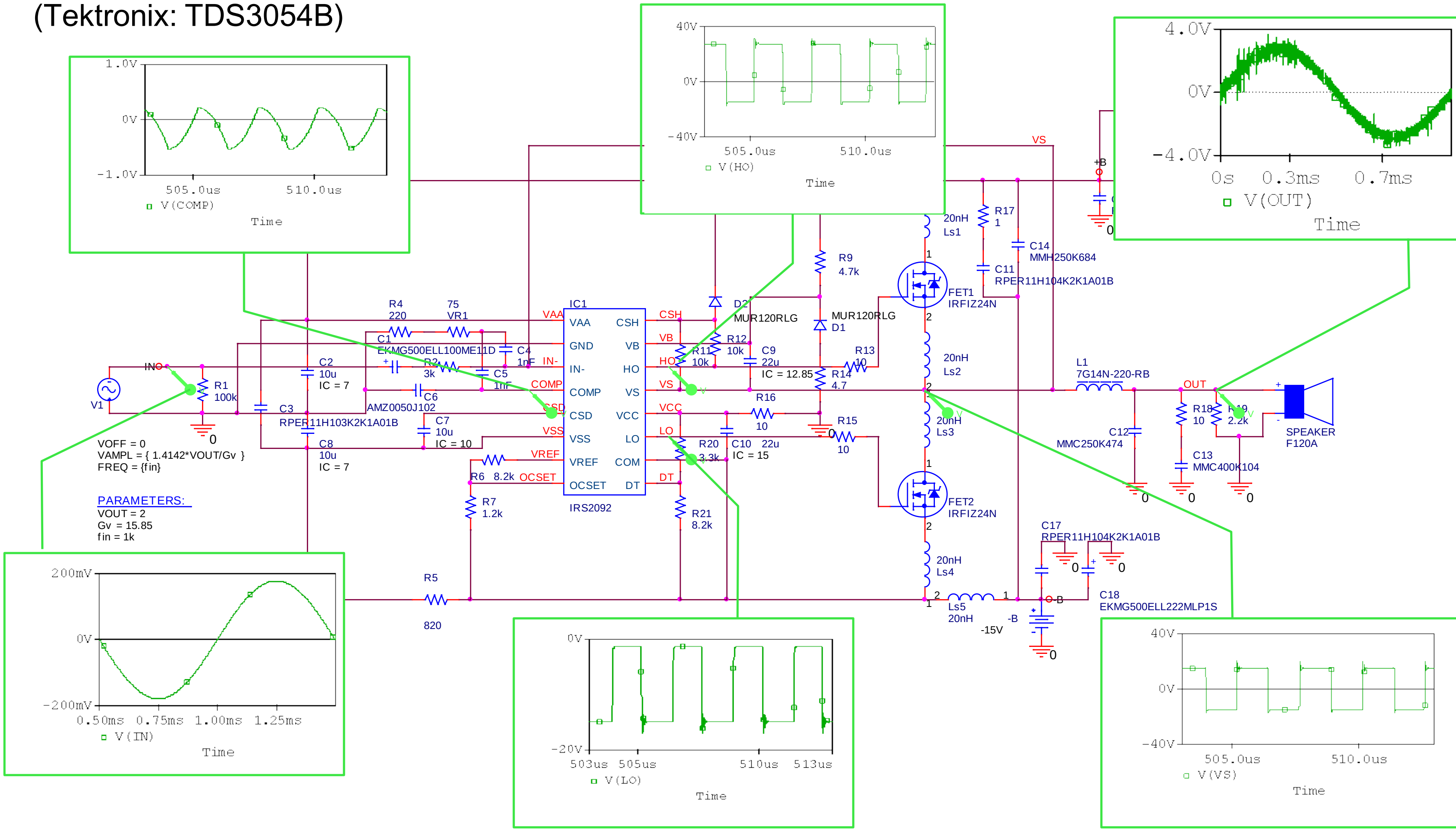
2. Waveforms Evaluation

Class D amplifier circuit are simulated and compared with measured waveforms from oscilloscope (Tektronix: TDS3054B)



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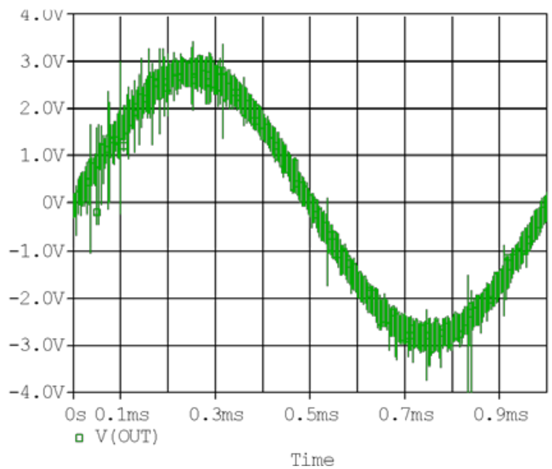
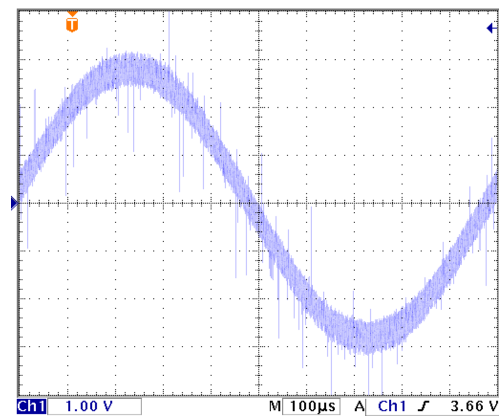
3. Simulated vs. Measured Waveform (1/3)

Simulated

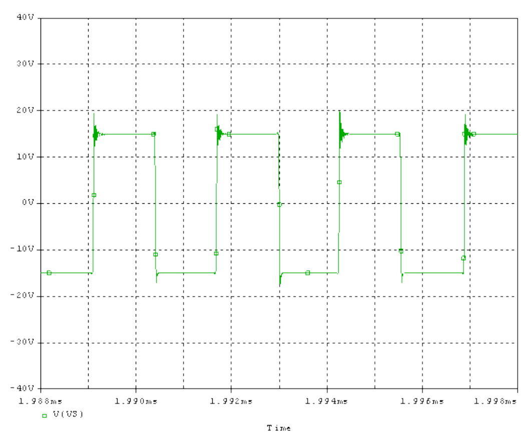
Measured

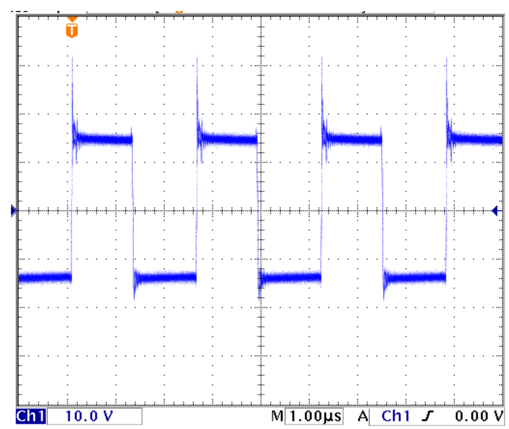
OUT





VS





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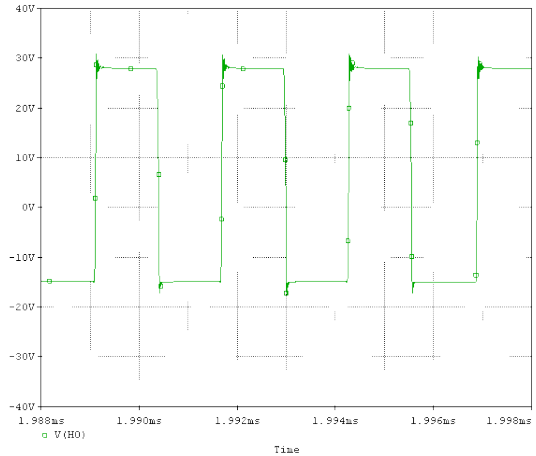
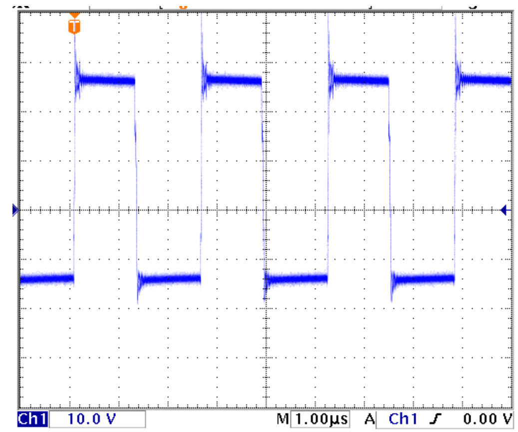
3. Simulated vs. Measured Waveform (2/3)

Simulated

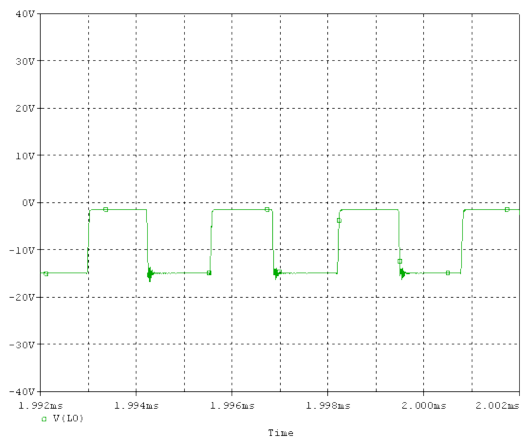
Measured

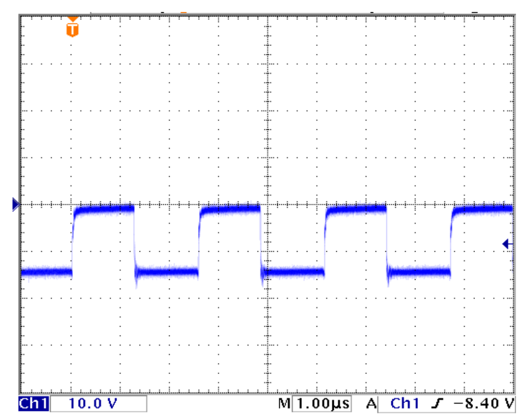
HO





LO





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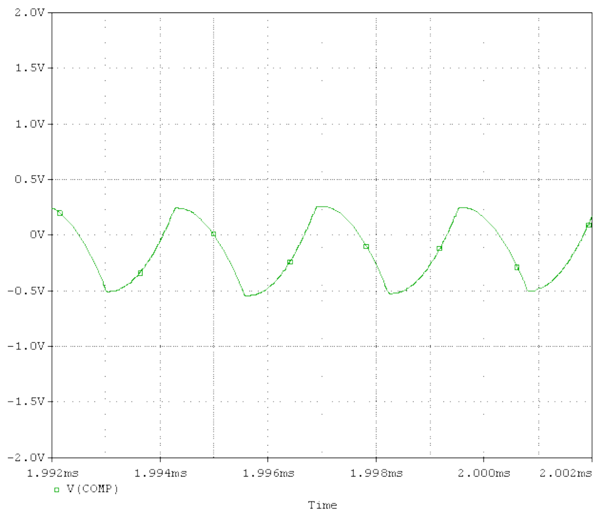
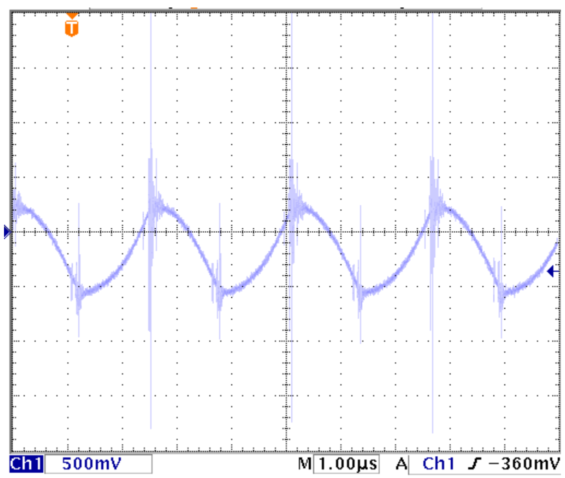
3. Simulated vs. Measured Waveform (3/3)

Simulated

Measured

COMP





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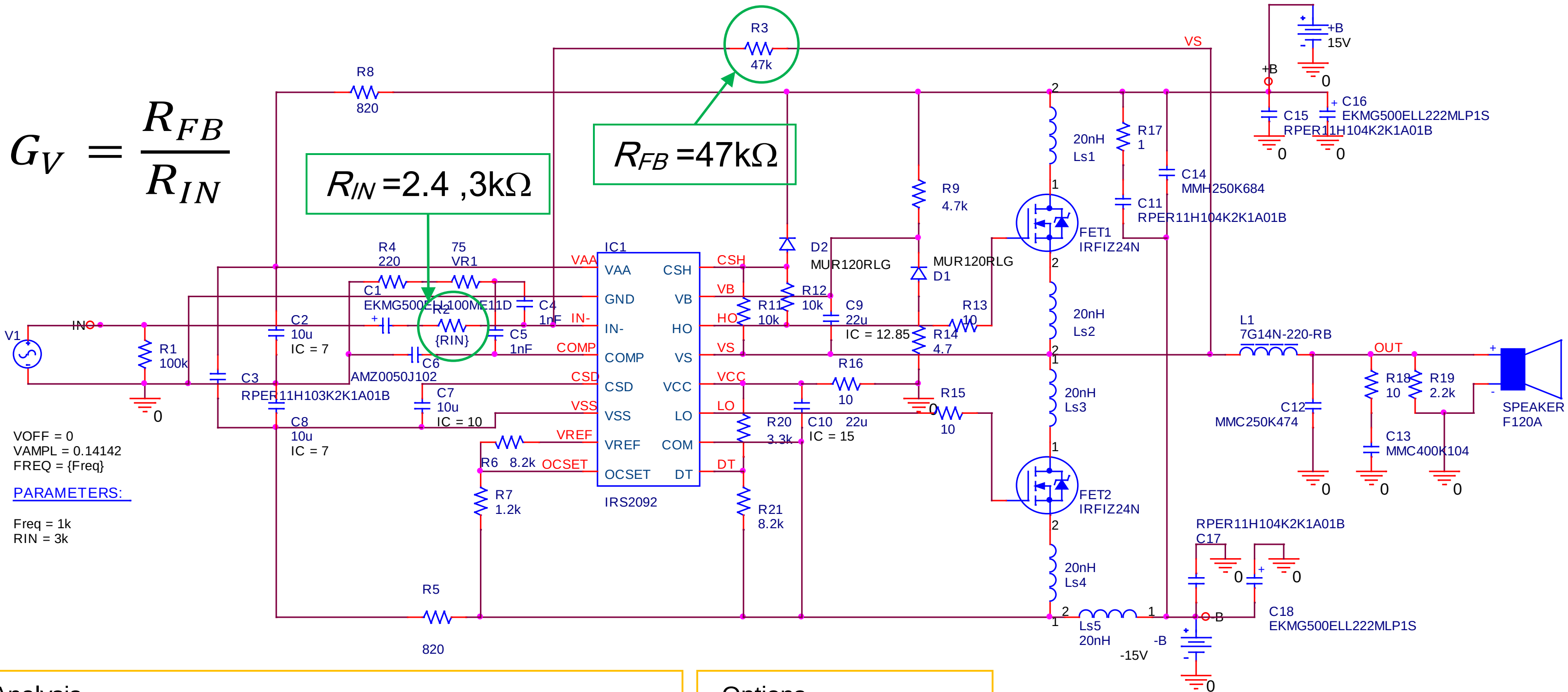
4. Voltage gain of the amplifier – G_V

$$G_V = \frac{R_{FB}}{R_{IN}}$$



Analysis
Time Domain (Transient)
Run to time: 1ms
Start saving data after: 100n
Maximum step size: 100n
☑ Skip the initial transient bias point calculation (SKIPBP)

Sweep variable
⦿ Global parameter: RIN
⦿ Value list: 2.4k, 3k

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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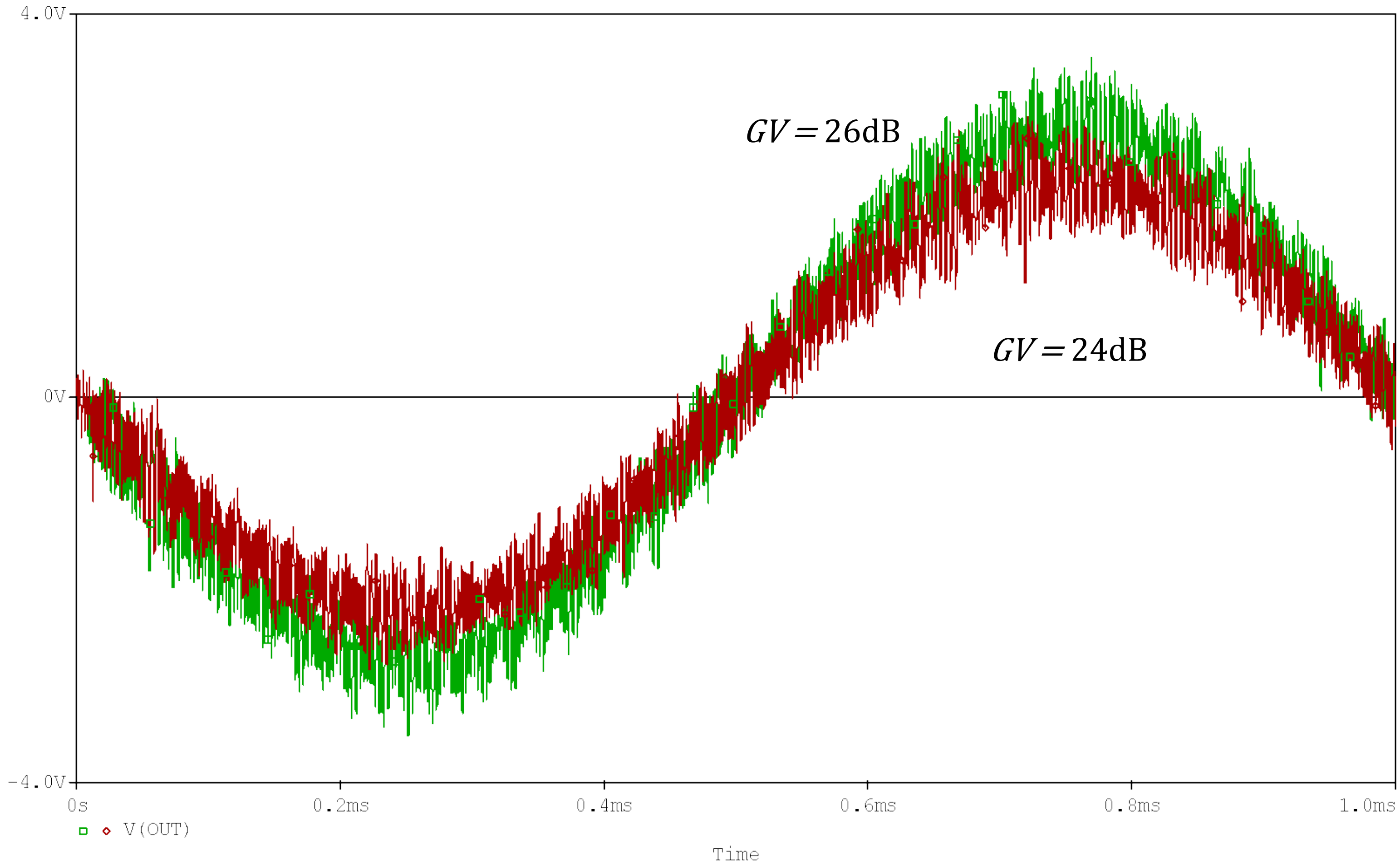
4. Voltage gain of the amplifier – G_V



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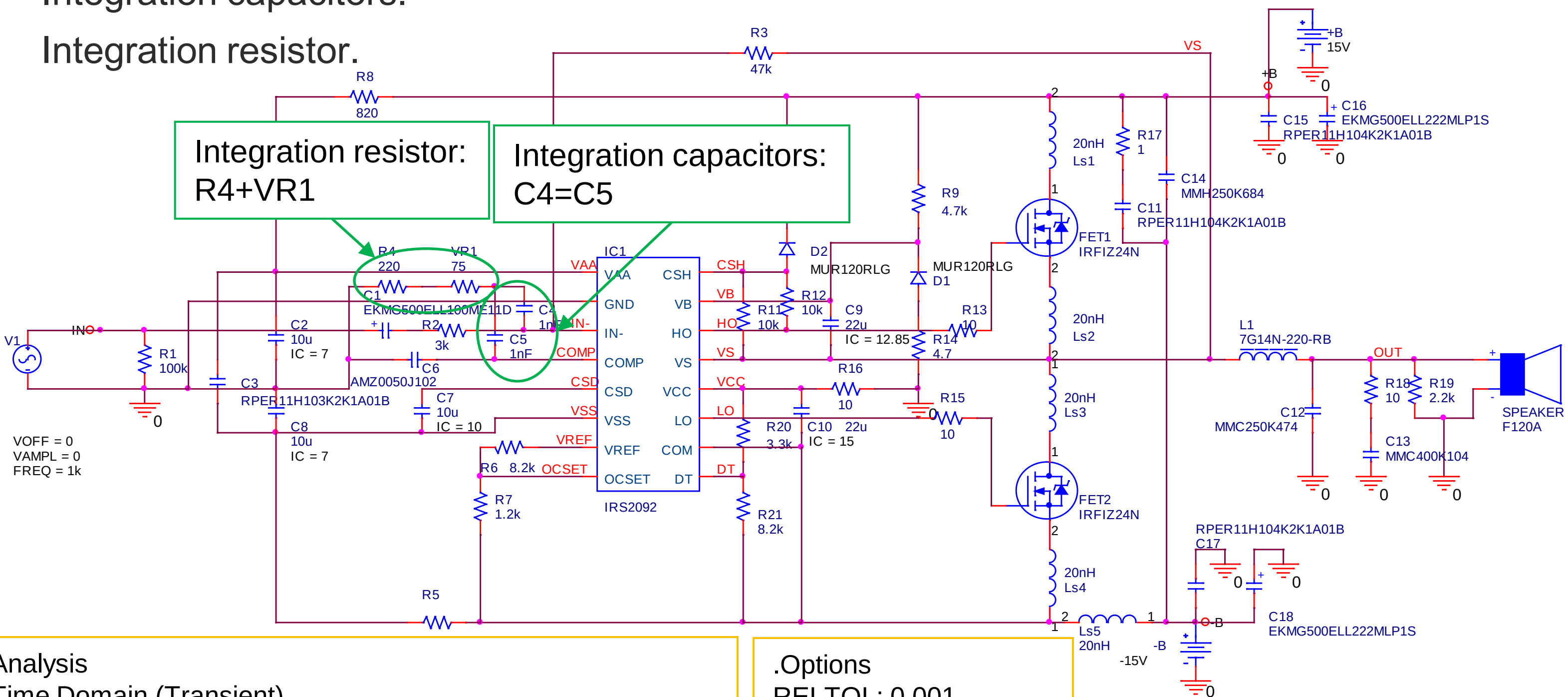
5. Self-Oscillating Frequency

Self oscillating frequency is design by setting the following items

- Integration capacitors.
- Integration resistor.



Analysis
Time Domain (Transient)
Run to time: 1ms
Start saving data after: 0.5m
Maximum step size: 40n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.001
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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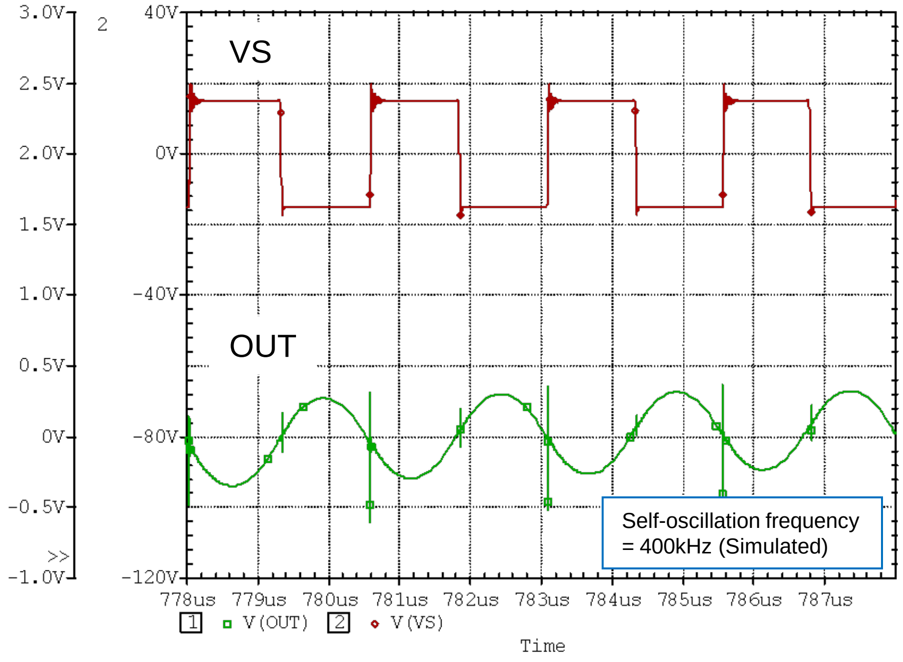
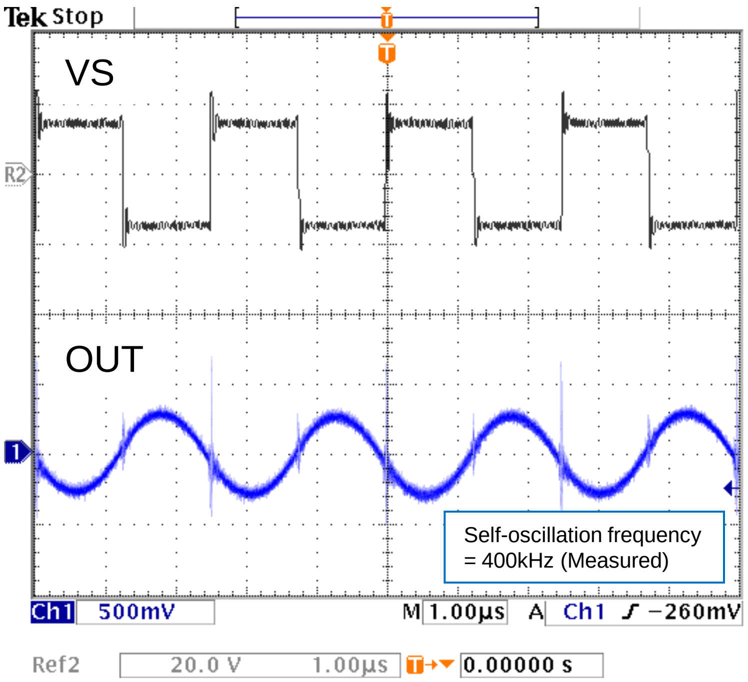
5. Self-Oscillating Frequency

Simulated



Measured



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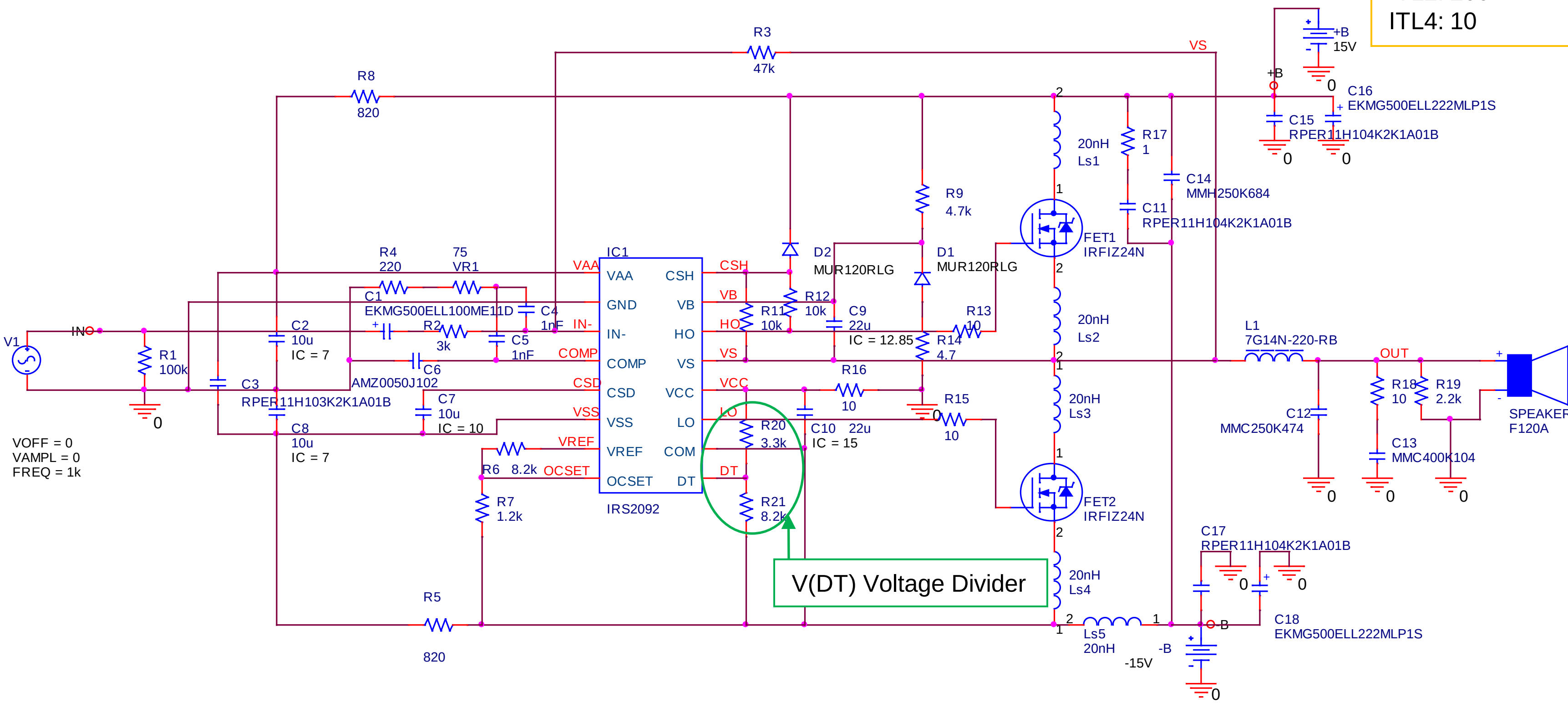
6. Dead-time

Dead-time Mode	R20	R21
DT1 (25ns)	3.3k	8.2k
DT2 (40ns)	5.6k	4.7k
DT3 (65ns)	8.2k	3.3k
DT4 (105ns)	-	< 10k

Analysis
Time Domain (Transient)
Run to time: 1ms
Start saving data after: 0.5m
Maximum step size: 40n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.001
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10



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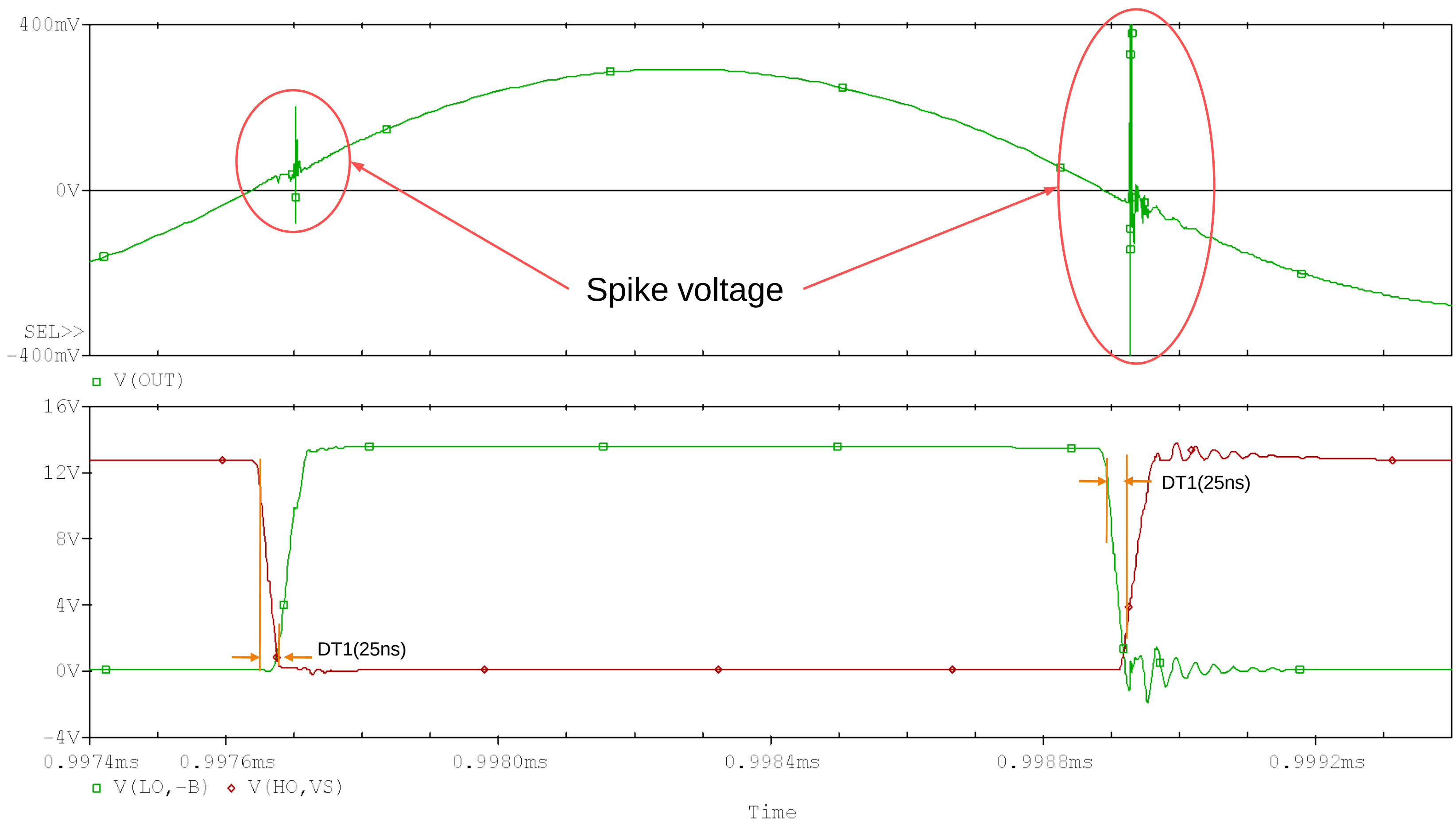
Dead-time DT1(25ns)



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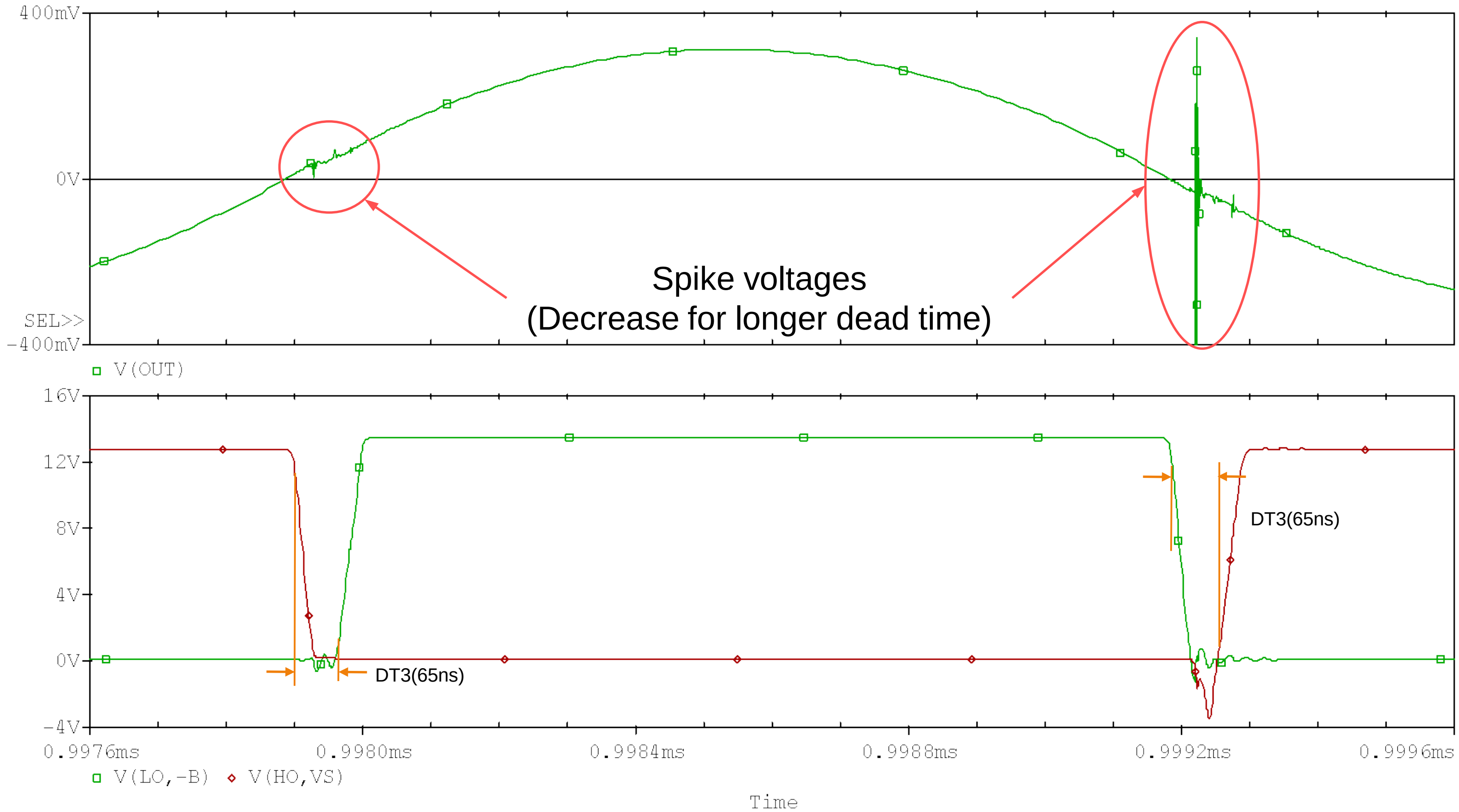
Dead-time DT3(65ns)



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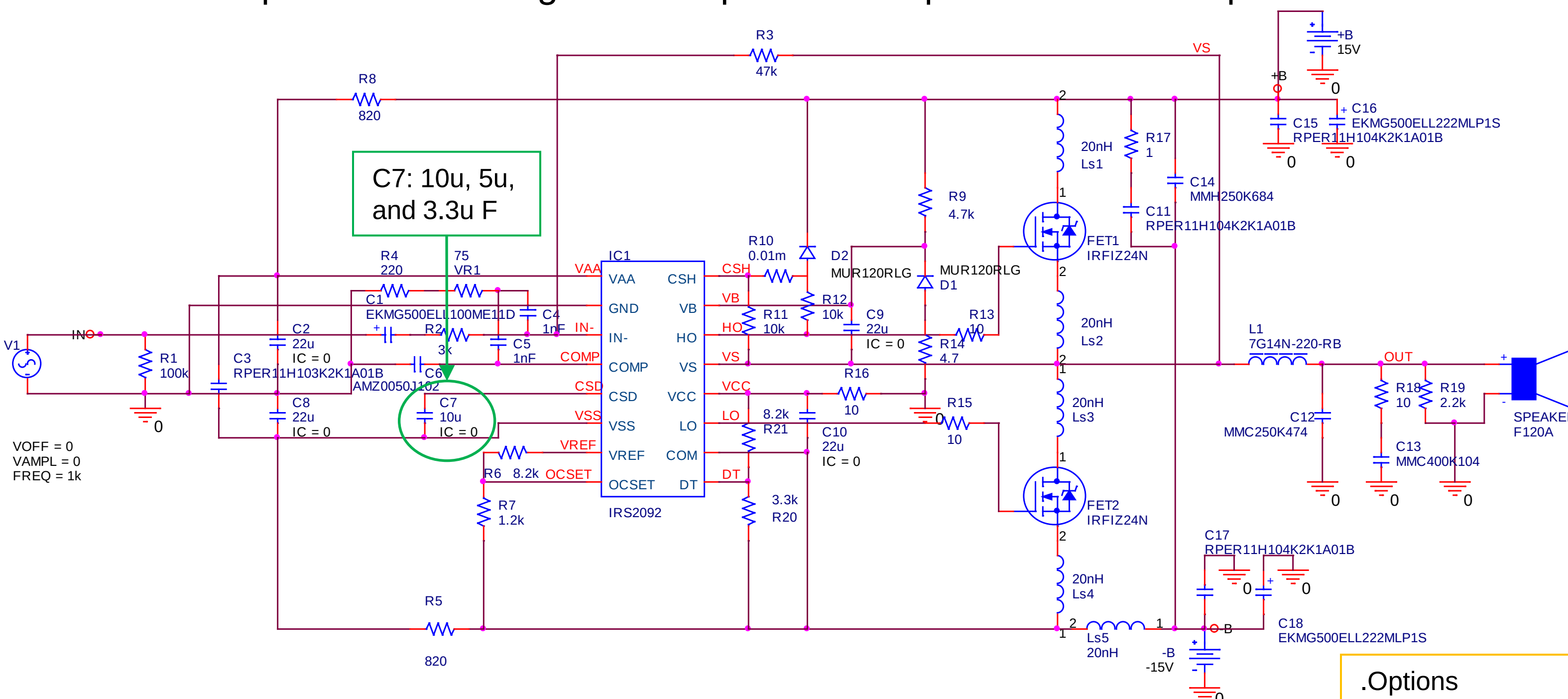
7. Turn-on transient

- Start-up sequencing is achieved through the charging of the CSD voltage (C7). Simulation will show how capacitors are charged to complete the sequence for each capacitance value.



Analysis
Time Domain (Transient)
Run to time: 975ms
Start saving data after: 100n
Maximum step size: 100u
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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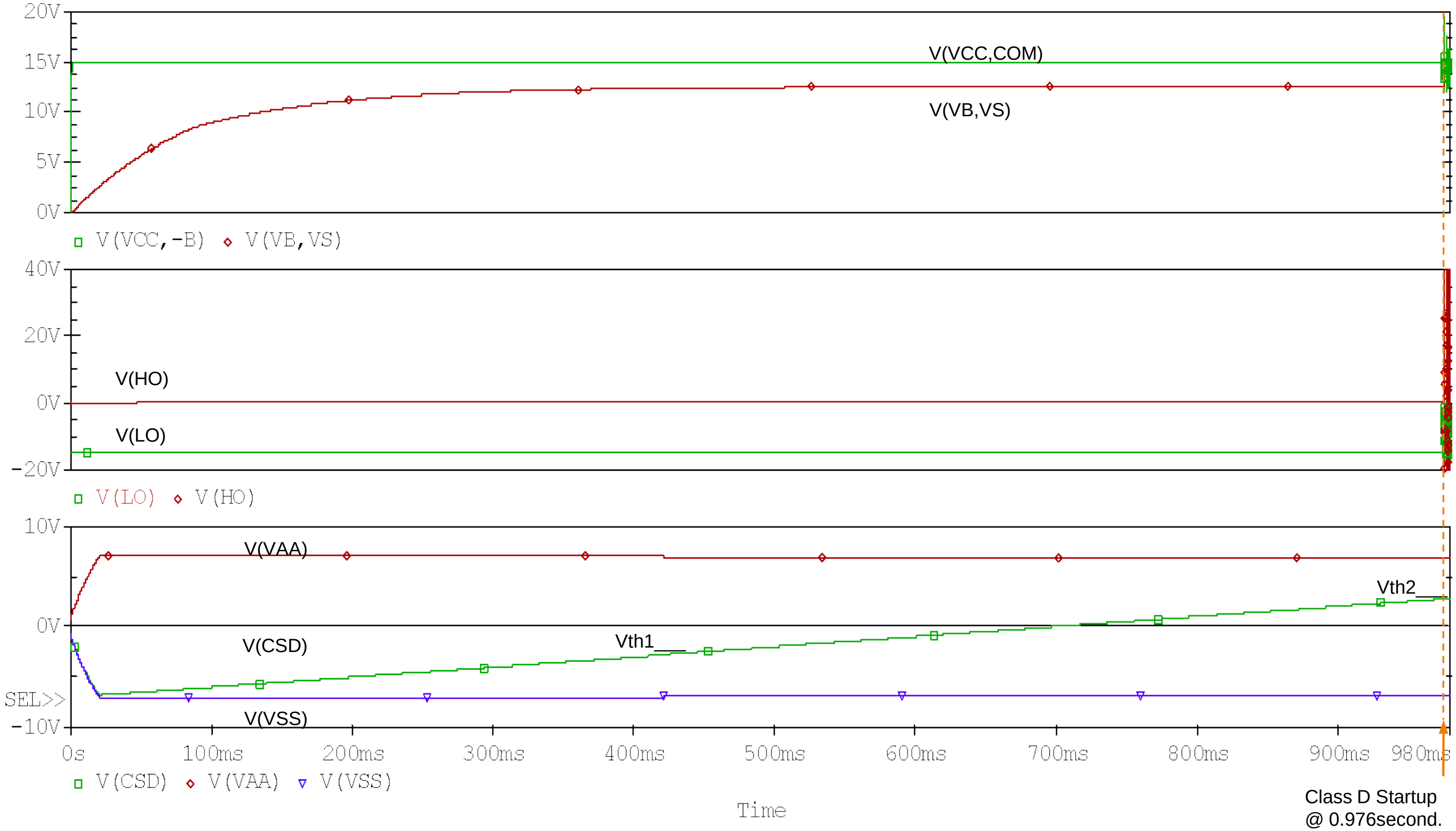
Turn-on transient: C7 = 10uF



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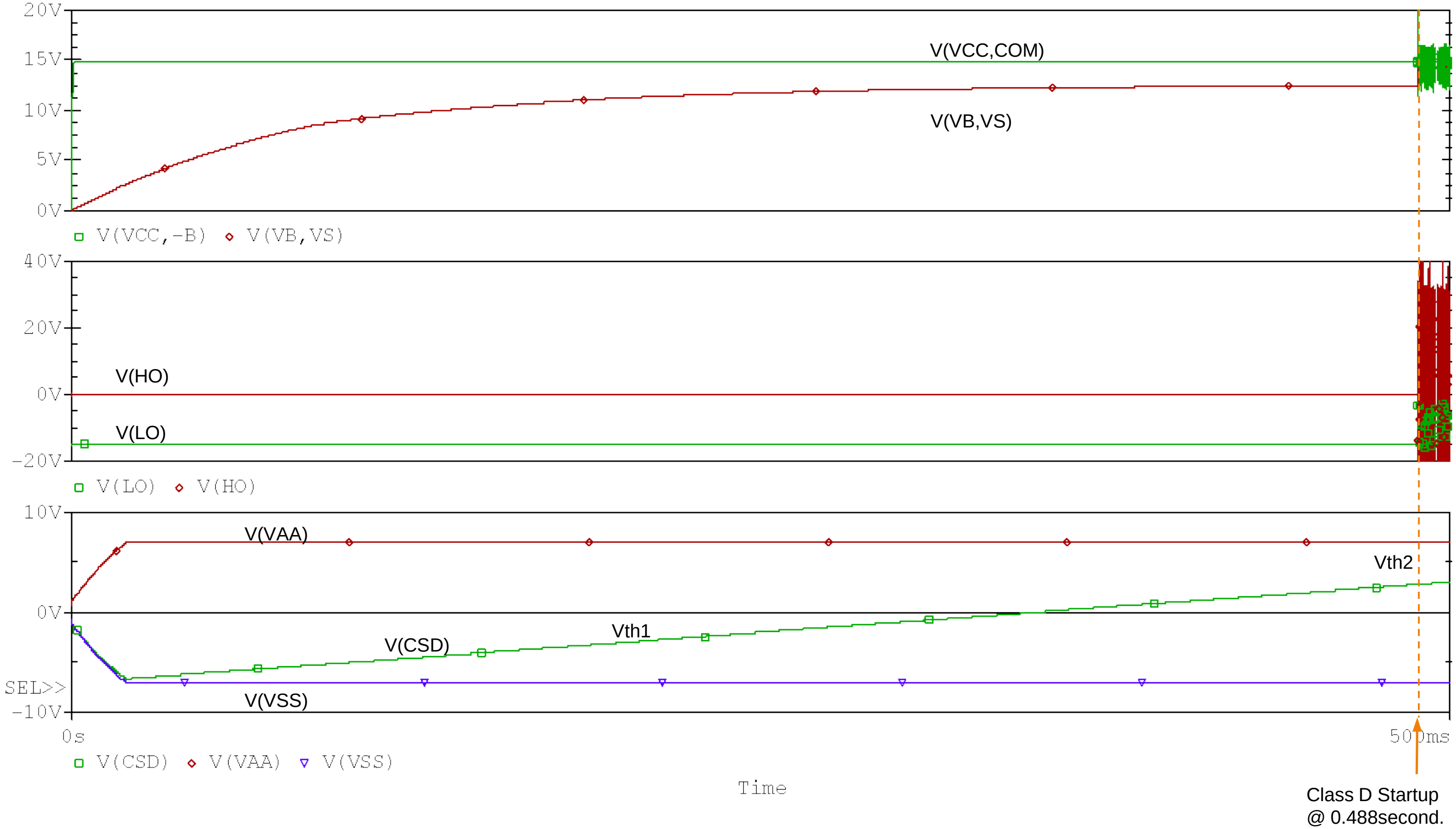
Turn-on transient: C7 = 5uF



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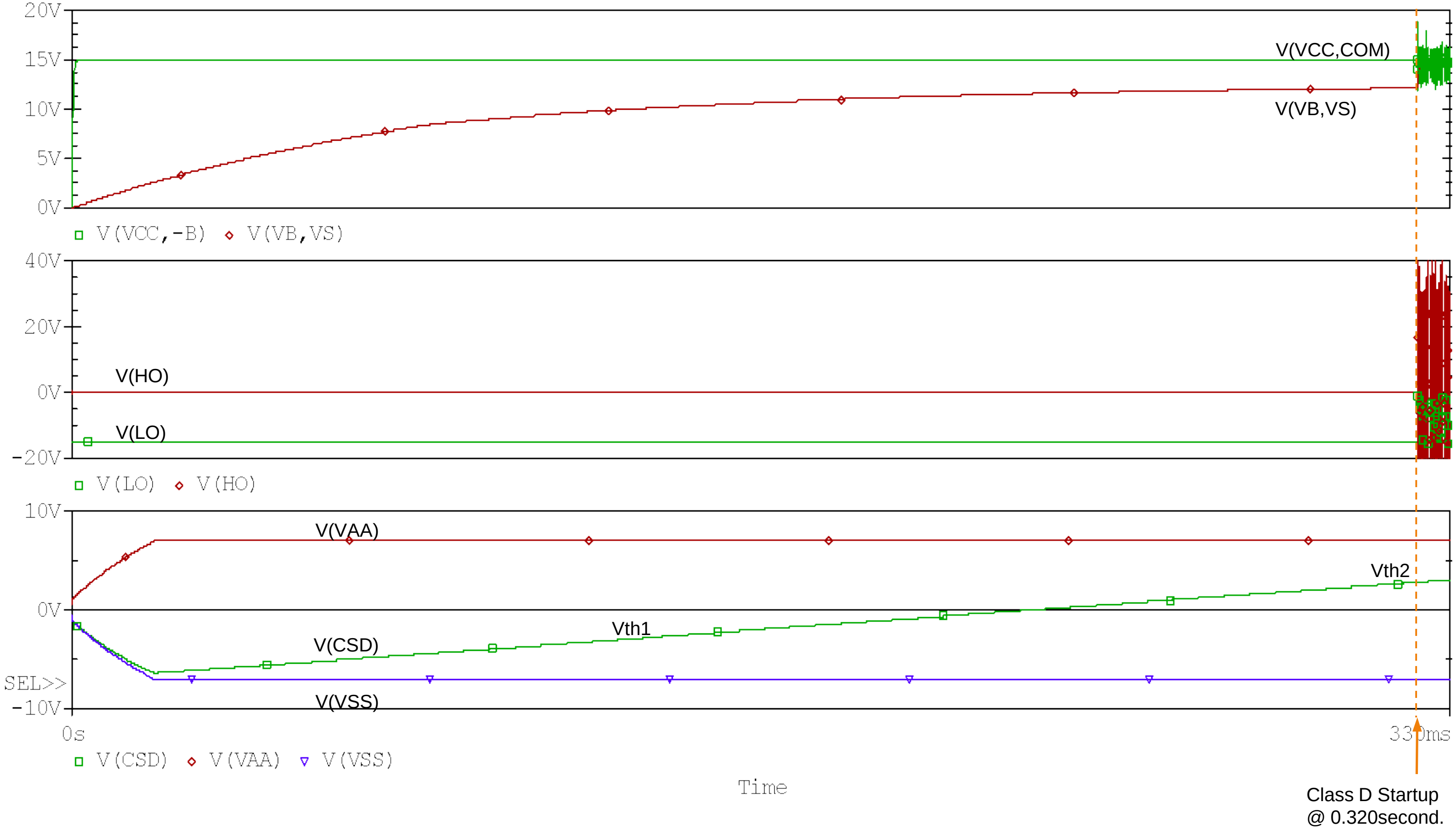
Turn-on transient: C7 = 3.3uF



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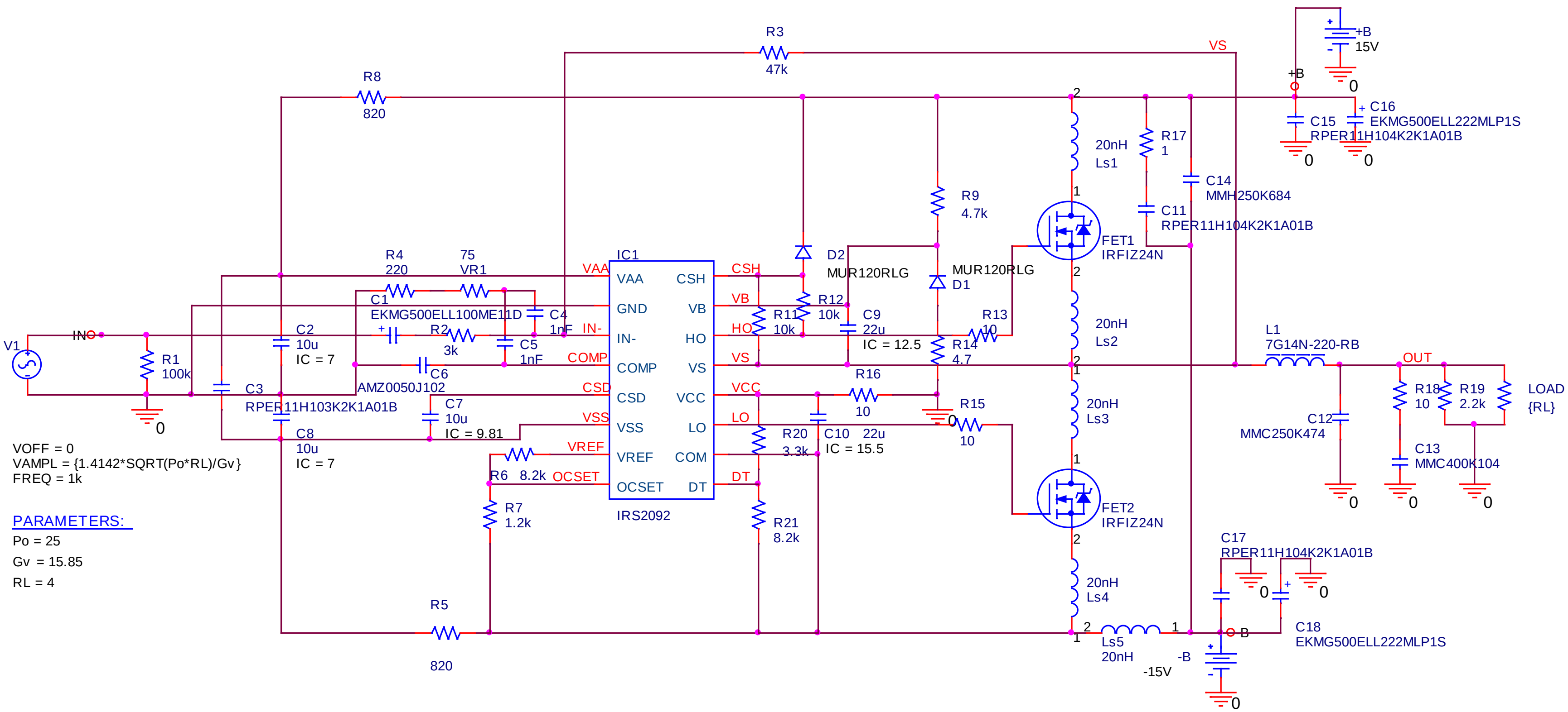
8. Components stress

- This simulation shows how voltage and current are applied to each components at the maximum load condition (25W,4ohm).



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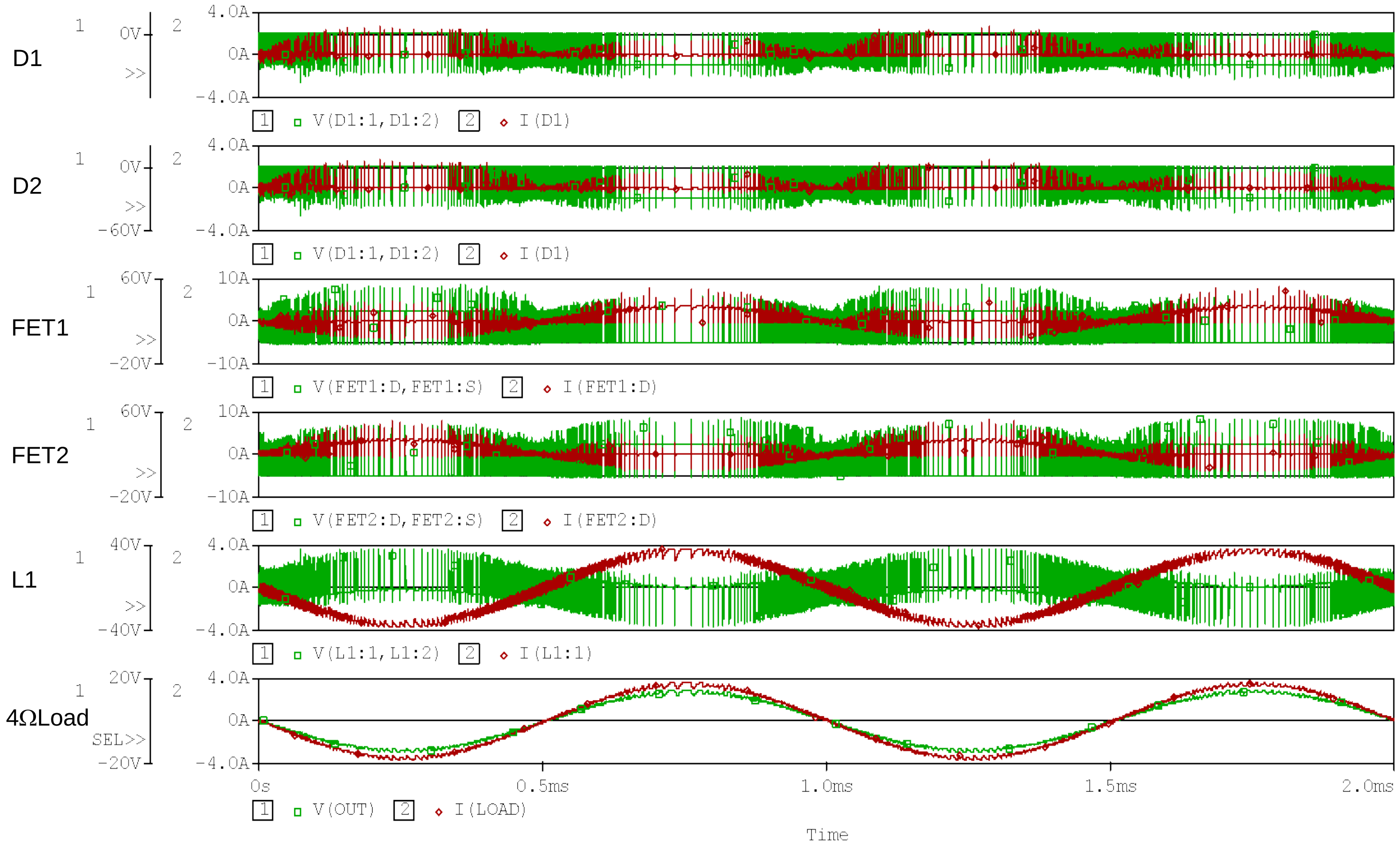
Components Stress Simulated Result for Diodes, FETs, Inductor, and 4ΩLoad



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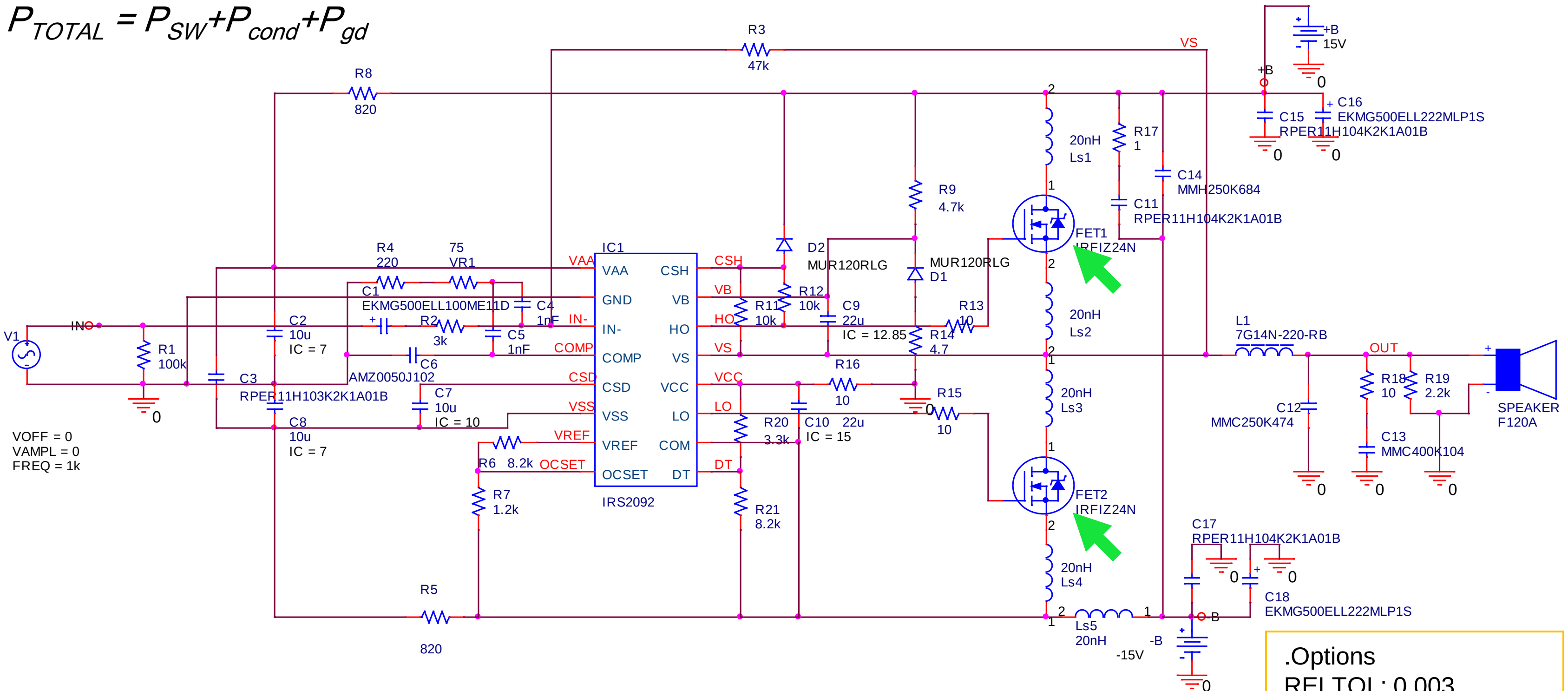
9. Power losses in the MOSFETs

The total power loss in MOSFET are given by:

$$P_{TOTAL} = P_{SW} + P_{cond} + P_{gd}$$



Analysis
Time Domain (Transient)
Run to time: 500us
Start saving data after: 100n
Maximum step size: 2n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.003
VNTOL: 1.0m
ABSTOL: 100n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 20

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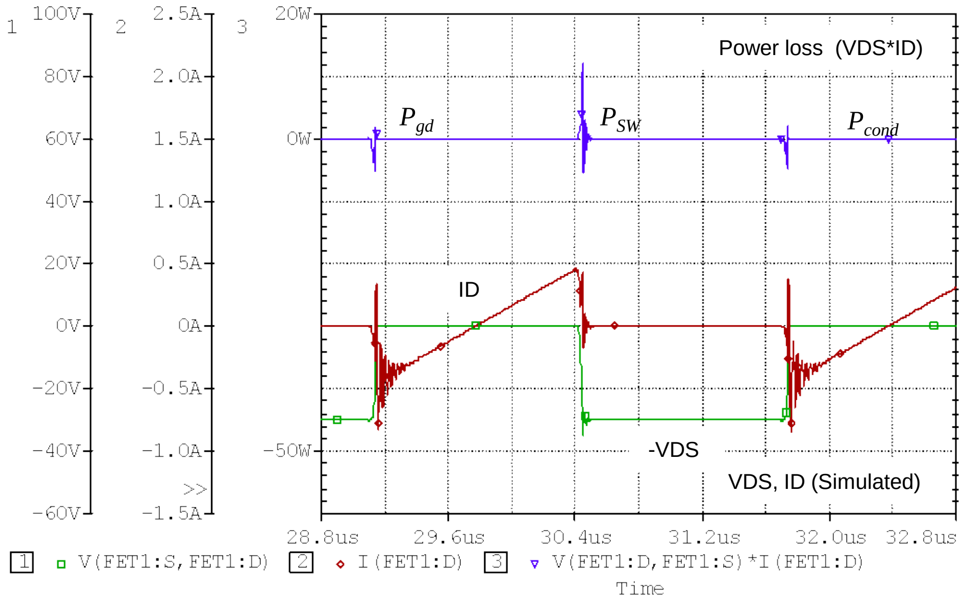
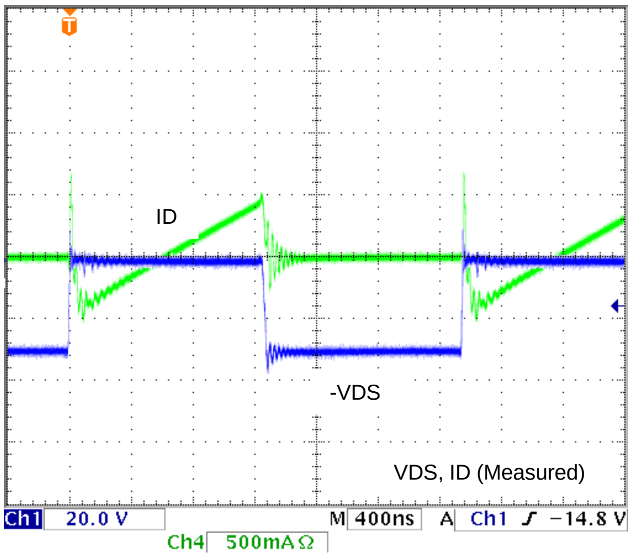
Power losses FET1(Standard Model)

FET1: ID and VDS are simulated and compared with scope (Tektronix: TDS3054B) waveforms

P_{SW}, P_{cond}, and P_{gd} are calculated by PSpice.





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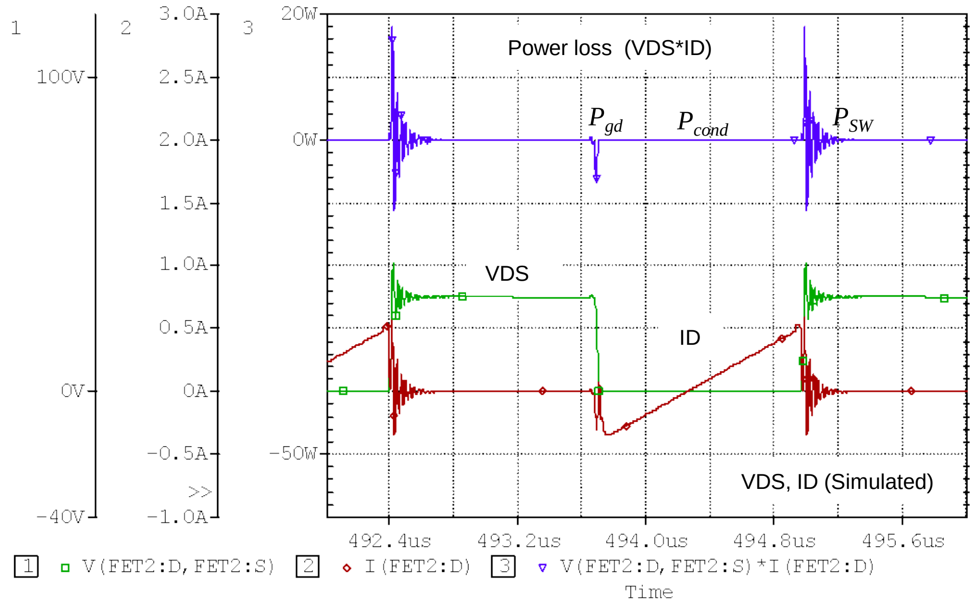
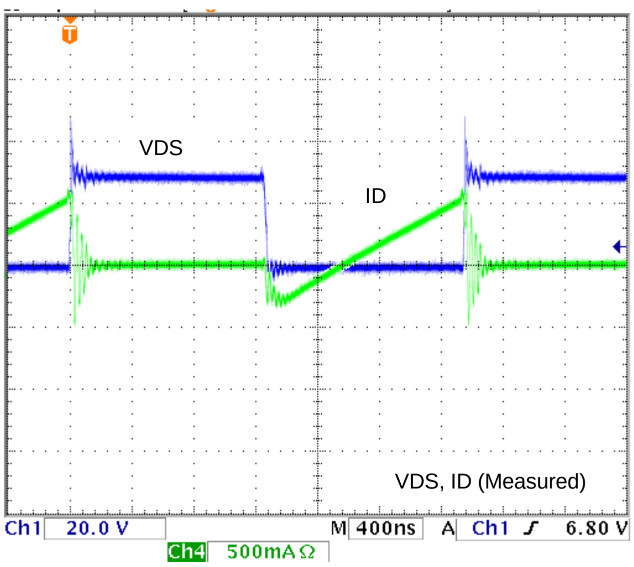
Power losses FET2(Standard Model)

FET2: ID and VDS are simulated and compared with scope (Tektronix: TDS3054B) waveforms

P_{SW} ,P_{cond} ,and P_{gd} are calculated by PSpice.





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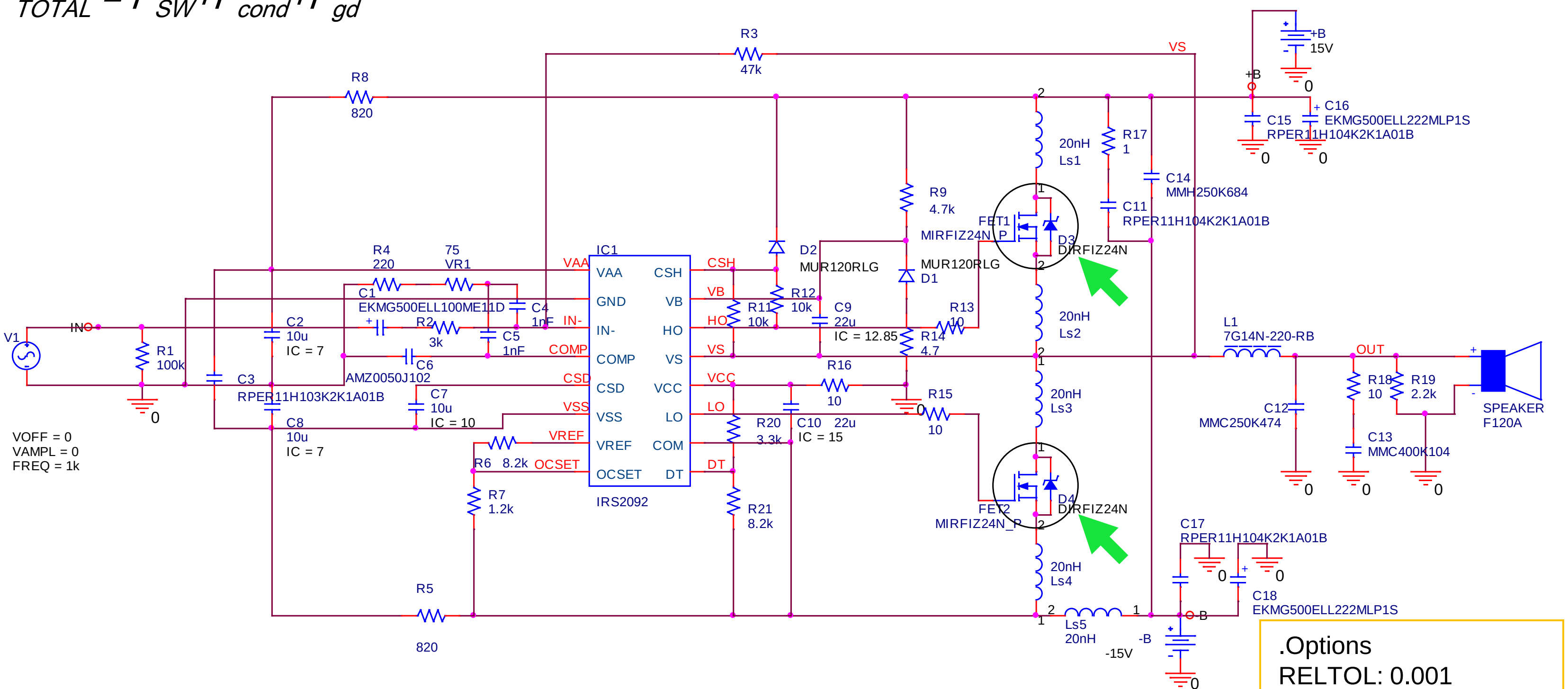
Power losses in the MOSFETs (Professional model)

The total power loss in MOSFET are given by:

$$P_{TOTAL} = P_{SW}+P_{cond}+P_{gd}$$



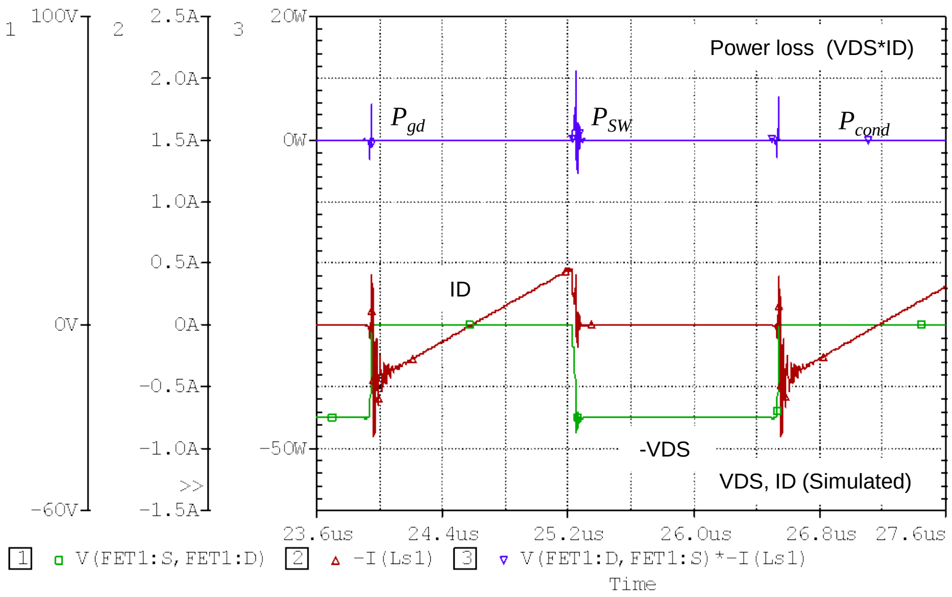
.Options
RELTOL: 0.001
VNTOL: 1.0m
ABSTOL: 100n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

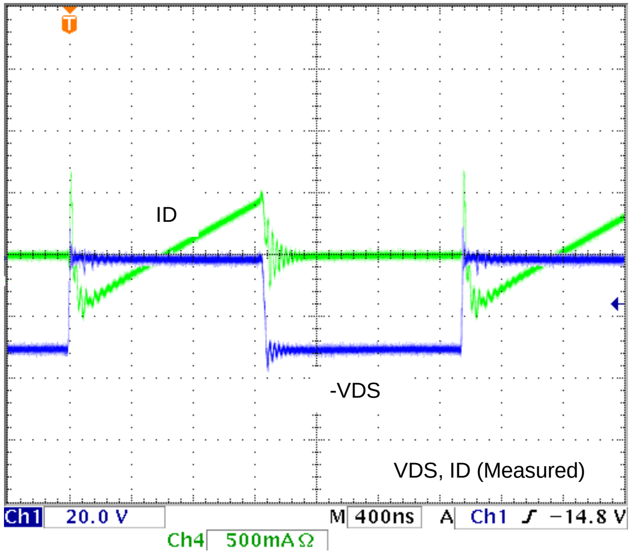
Analysis
Time Domain (Transient)
Run to time: 500us
Start saving data after: 100n
Maximum step size: 2n
☑ Skip the initial transient bias point calculation (SKIPBP)

Power losses FET1(Professional Model)

FET1: ID and VDS are simulated and compared with scope (Tektronix: TDS3054B) waveforms

P_{SW} ,P_{cond} ,and P_{gd} are calculated by PSpice.





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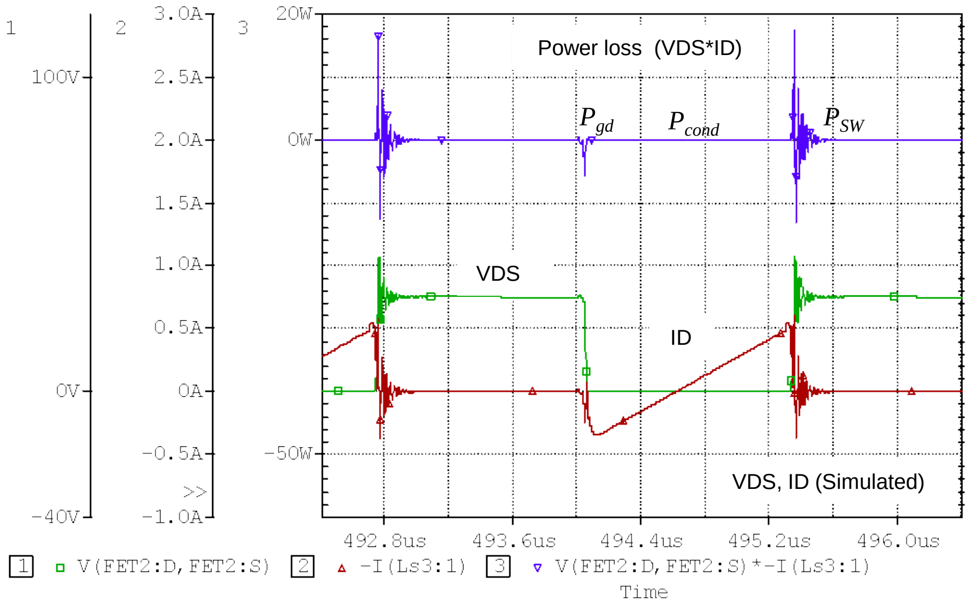
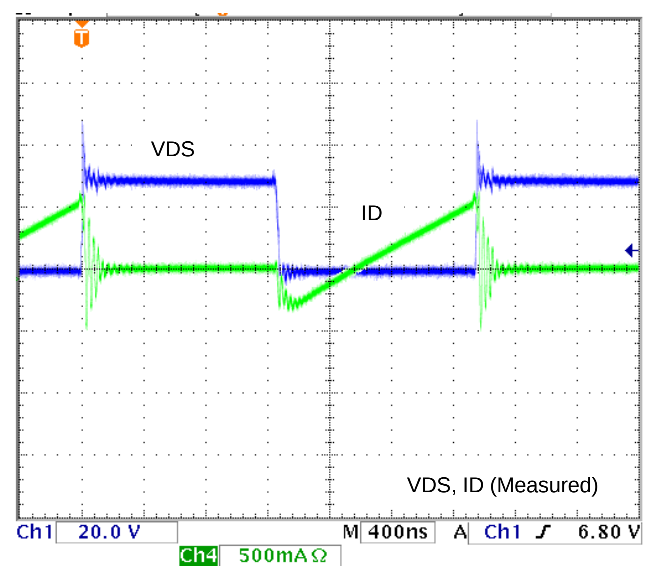
Power losses FET2(Professional Model)

FET2: ID and VDS are simulated and compared with scope (Tektronix: TDS3054B) waveforms

P_{SW} ,P_{cond} ,and P_{gd} are calculated by PSpice.





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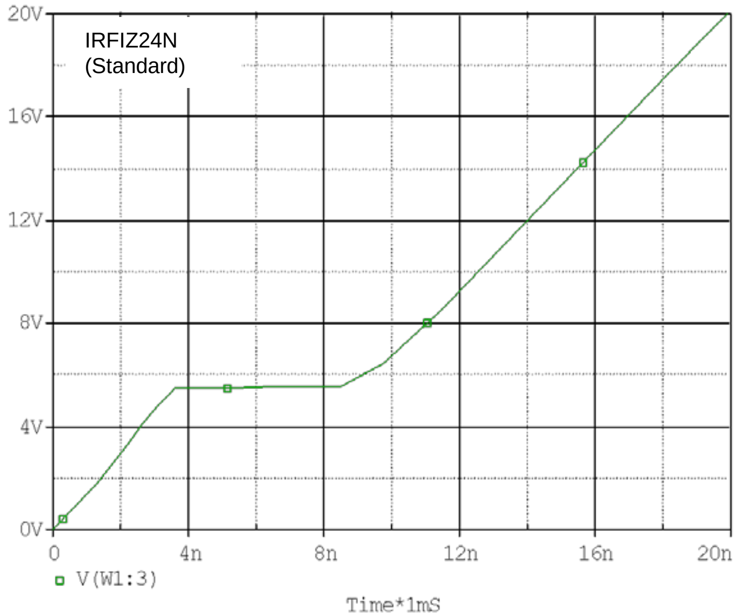
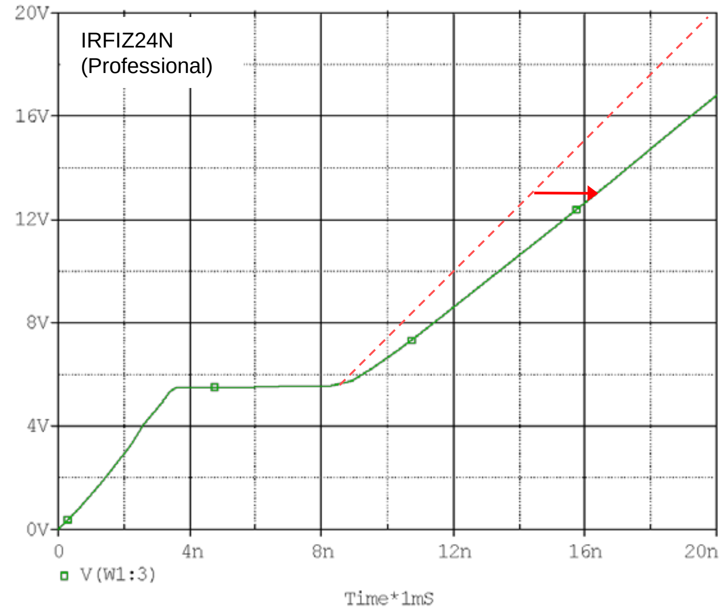
FET: IRFIZ24N Qg Standard vs. Professional Model

- Gate charge characteristics in Professional model has more accurate results than standard model.





V_{DD}=44V,I_D=10A ,V_{GS}=10V	Measurement	Simulation	Error (%)
Standard Model: Qg(nc)	13.400	12.543	-6.396
Professional Model: Qg(nc)	13.400	13.409	0.067

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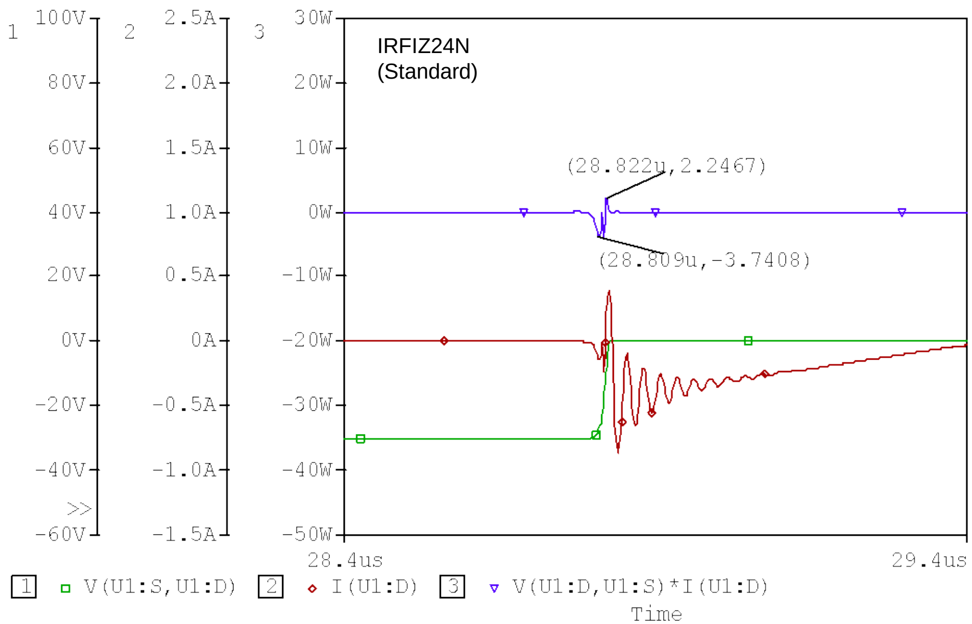
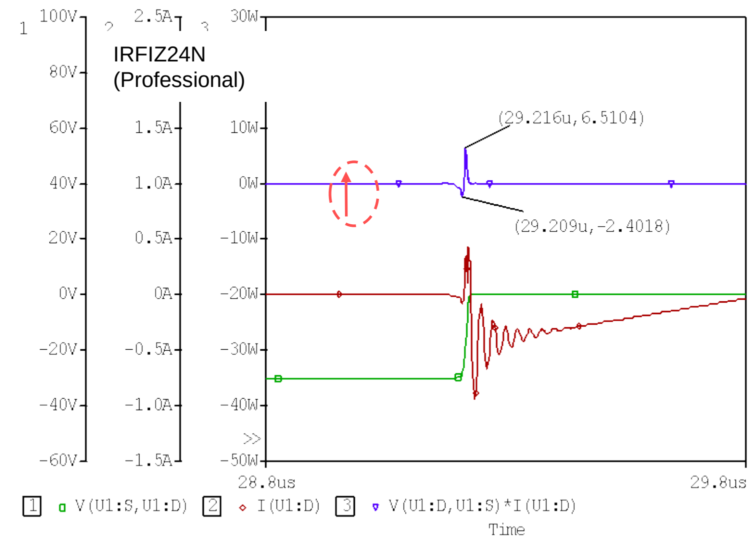
FET: IRFIZ24N P_{gd} Standard vs. Professional Model

- Simulated P_{gd} ,Standard model compared to Professional model ,shows some different result caused by different Qg characteristics of the models.





※ Professional model requires more simulation time and might cause some convergence error.

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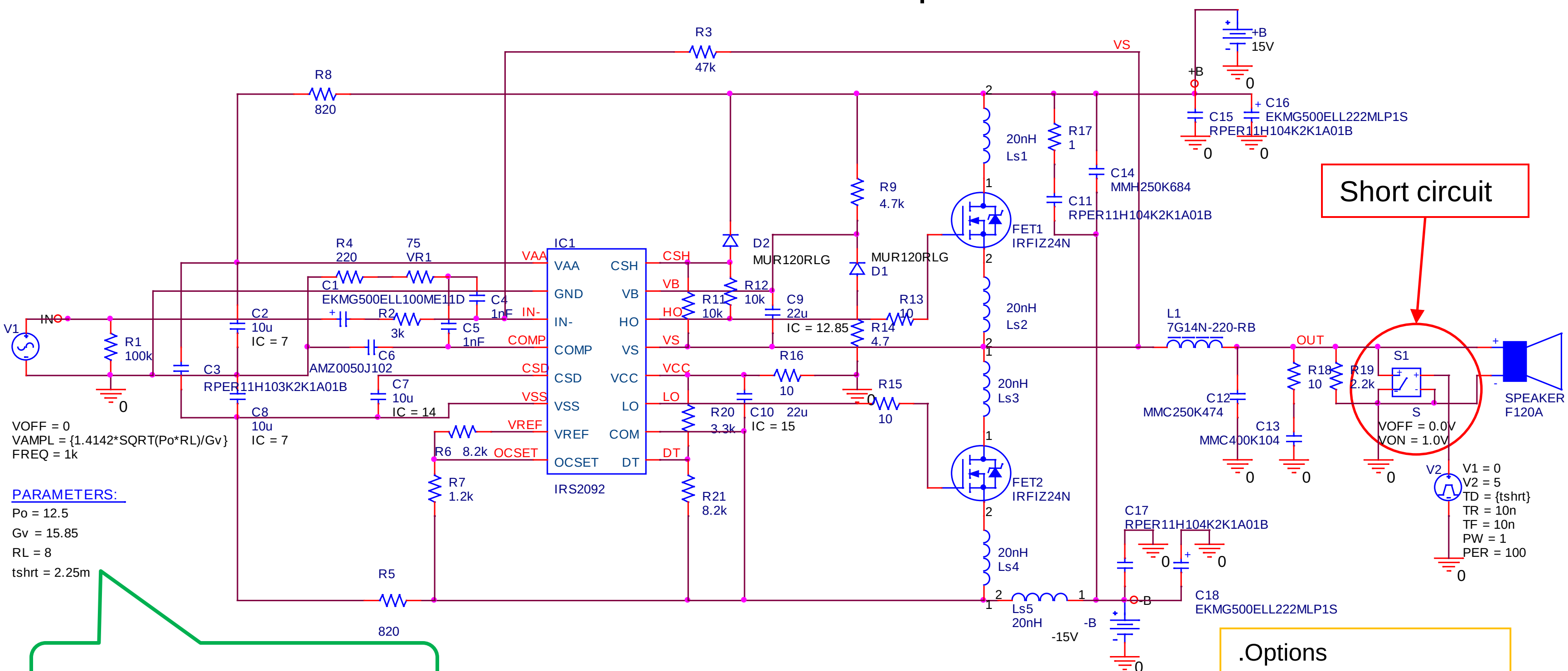
10. Short circuit vs. switching output shutdown

- This simulation will show how the IRS2092 responds to a short circuit condition.



Short circuit at 2.25ms.

Analysis
Time Domain (Transient)
Run to time: 4ms
Start saving data after: 100n
Maximum step size: 100n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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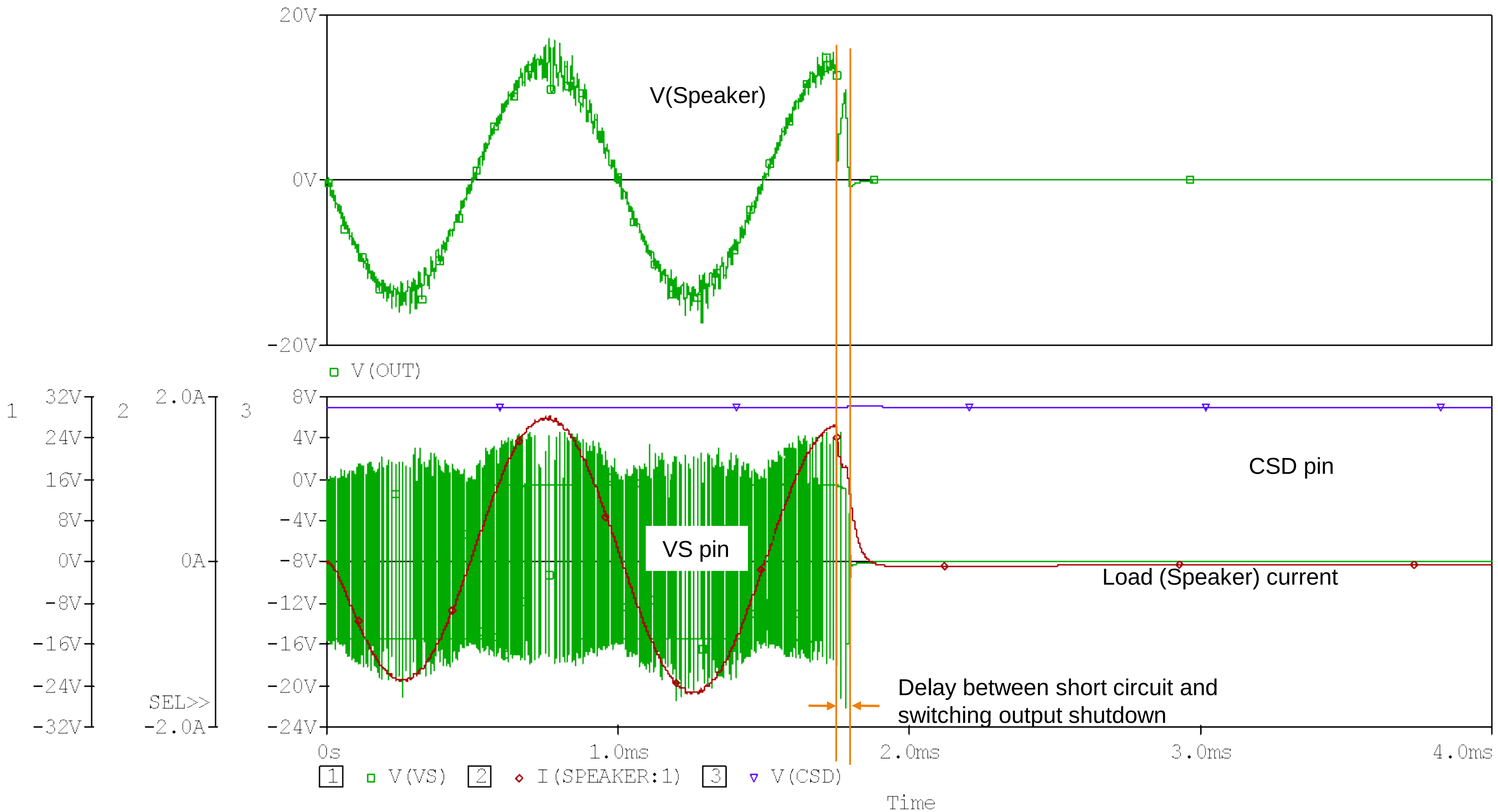
Short Circuit vs. Switching Output Shutdown (Positive Side)



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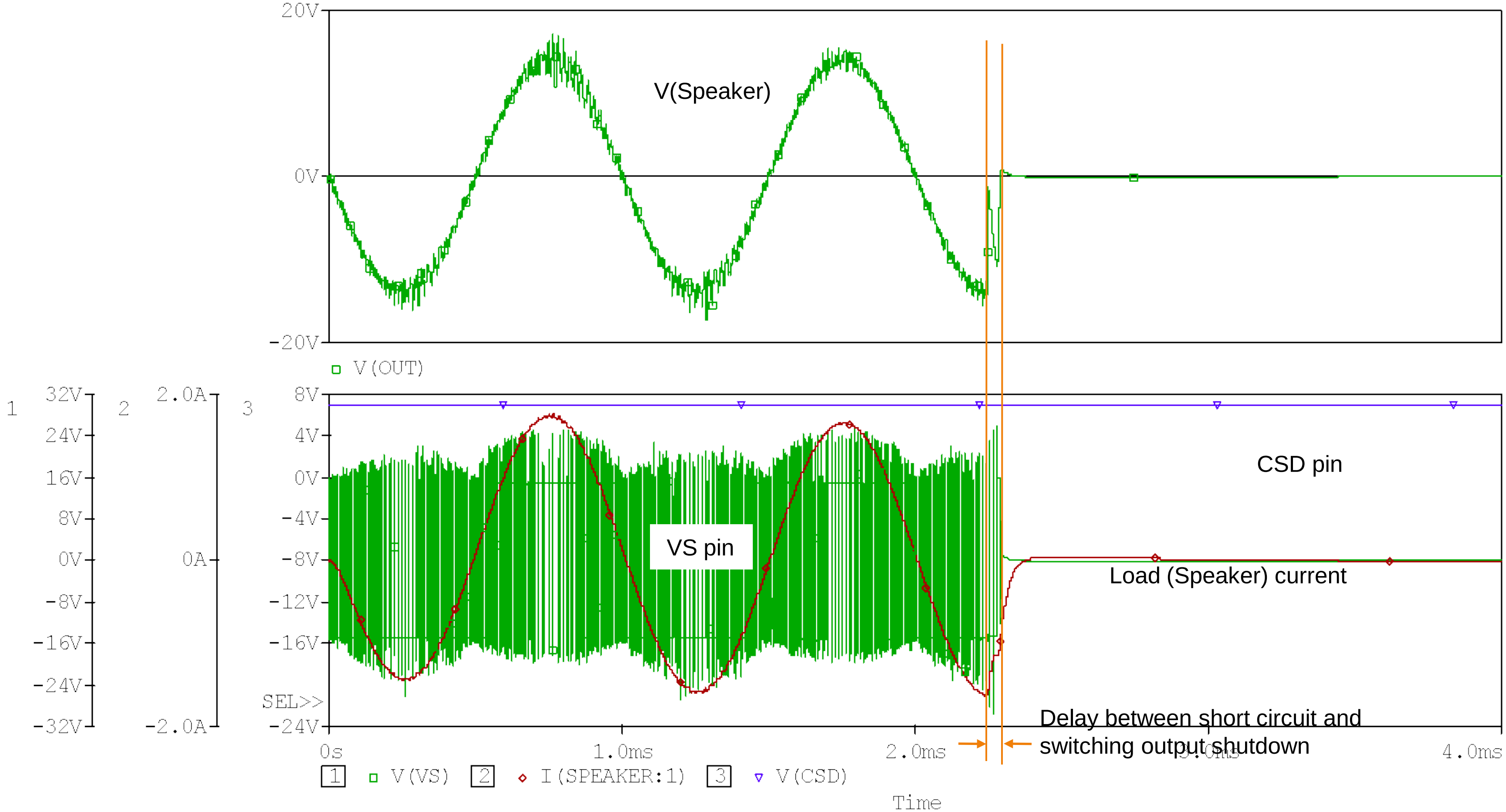
Short Circuit vs. Switching Output Shutdown (Negative Side)



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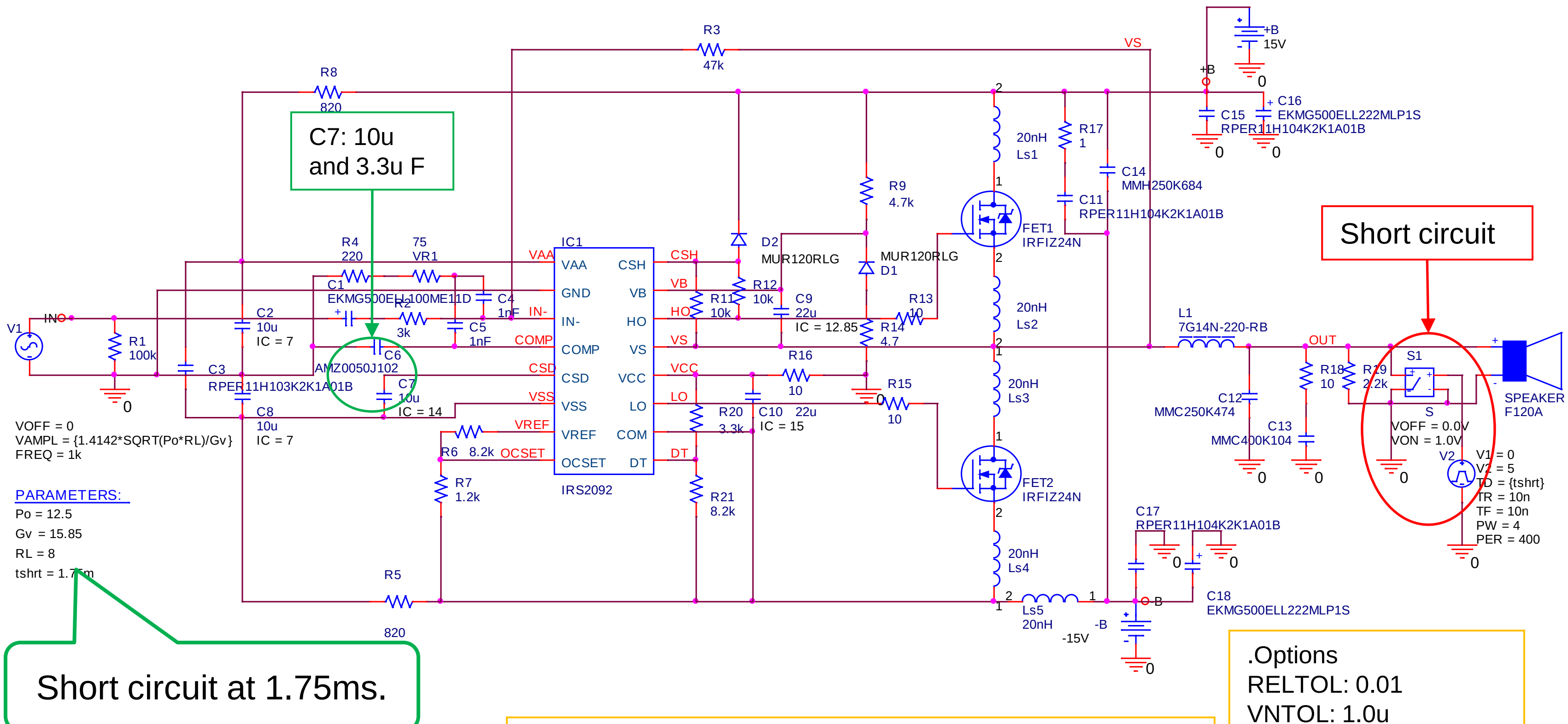
11. Short Circuit Response

- This simulation will show how the IRS2092 responds to a short circuit condition.



Analysis
Time Domain (Transient)
Run to time: 1.25s
Start saving data after: 100n
Maximum step size: 100u
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.01
VNTOL: 1.0u
ABSTOL: 1n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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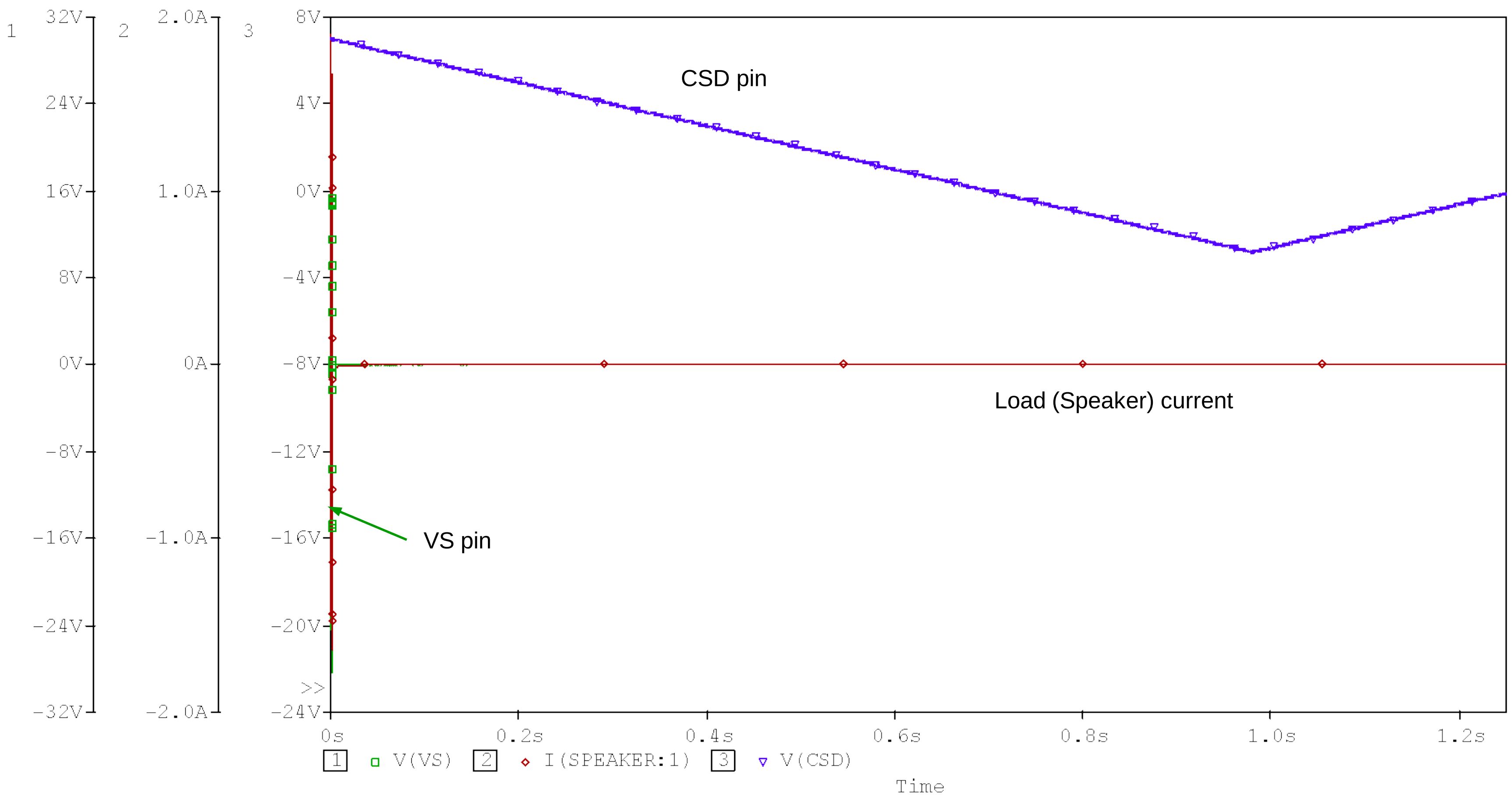
Short Circuit Response: C7 = 10uF



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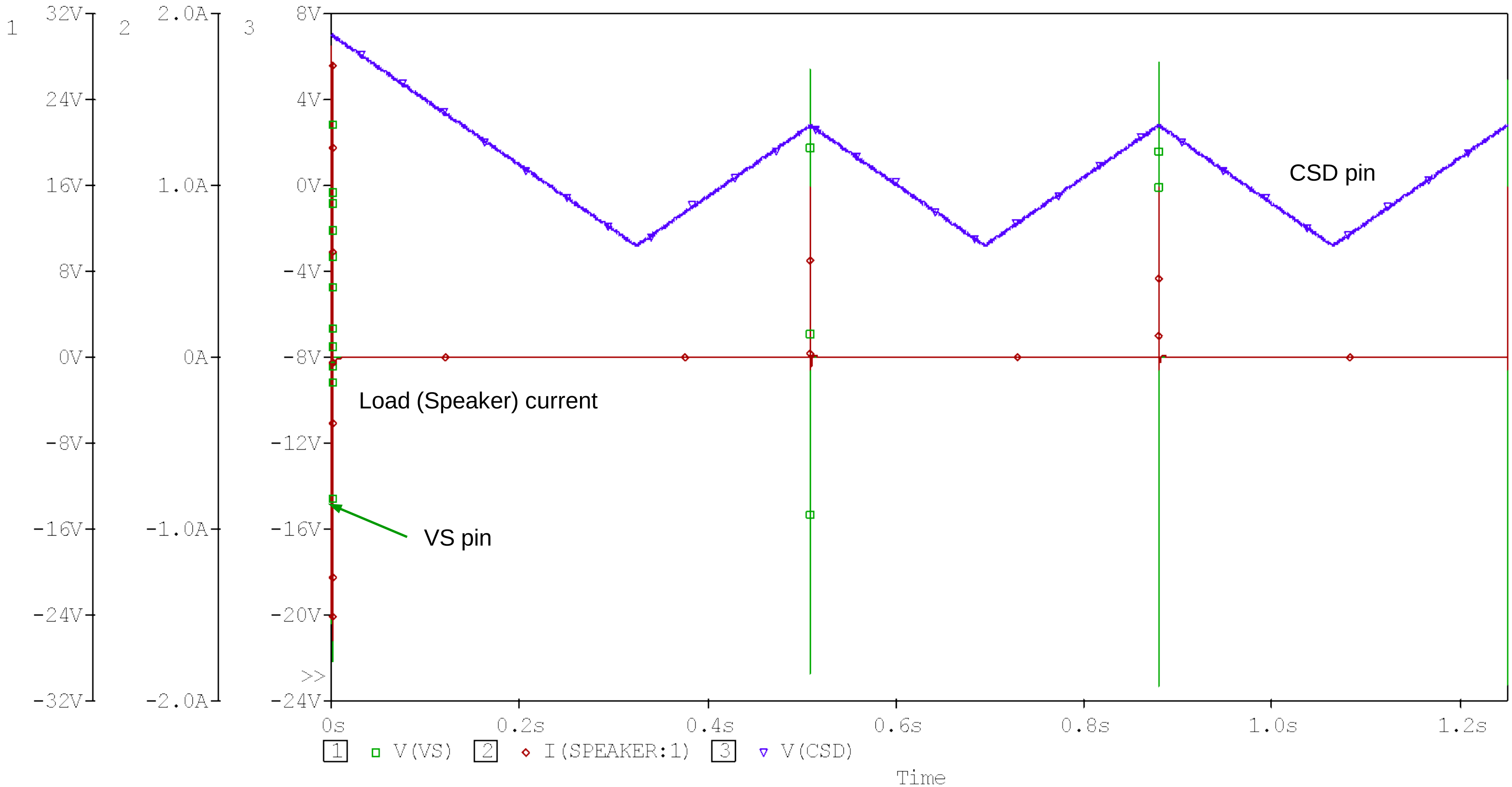
Short Circuit Response: C7 = 3.3uF



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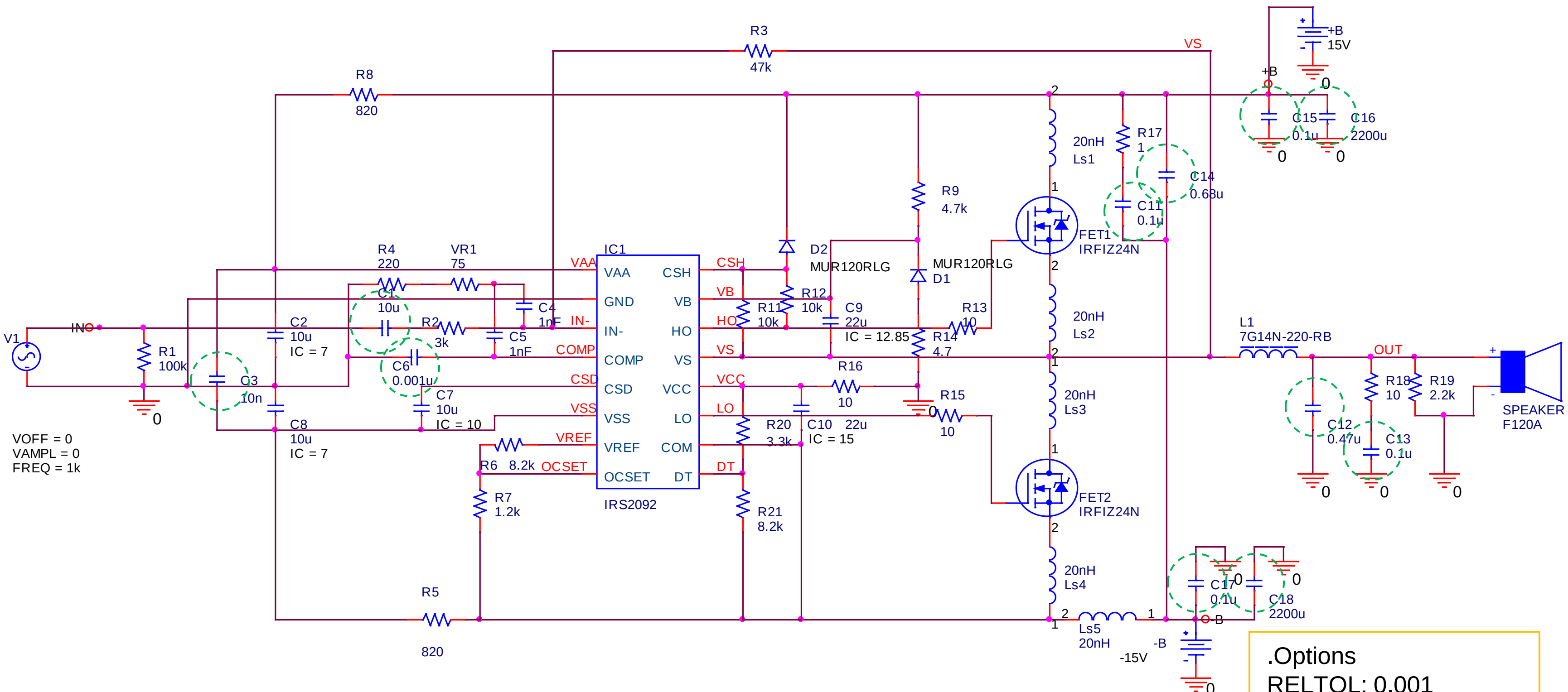
12. Capacitor models

- Capacitor models are needed for the simulation to include spike voltage.



Analysis
Time Domain (Transient)
Run to time: 1ms
Start saving data after: 0.5m
Maximum step size: 40n
☑ Skip the initial transient bias point calculation (SKIPBP)

.Options
RELTOL: 0.001
VNTOL: 1.0u
ABSTOL: 1.0n
CHGTOL: 0.01p
GMIN: 1.0E-12
ITL1: 500
ITL2: 200
ITL4: 10

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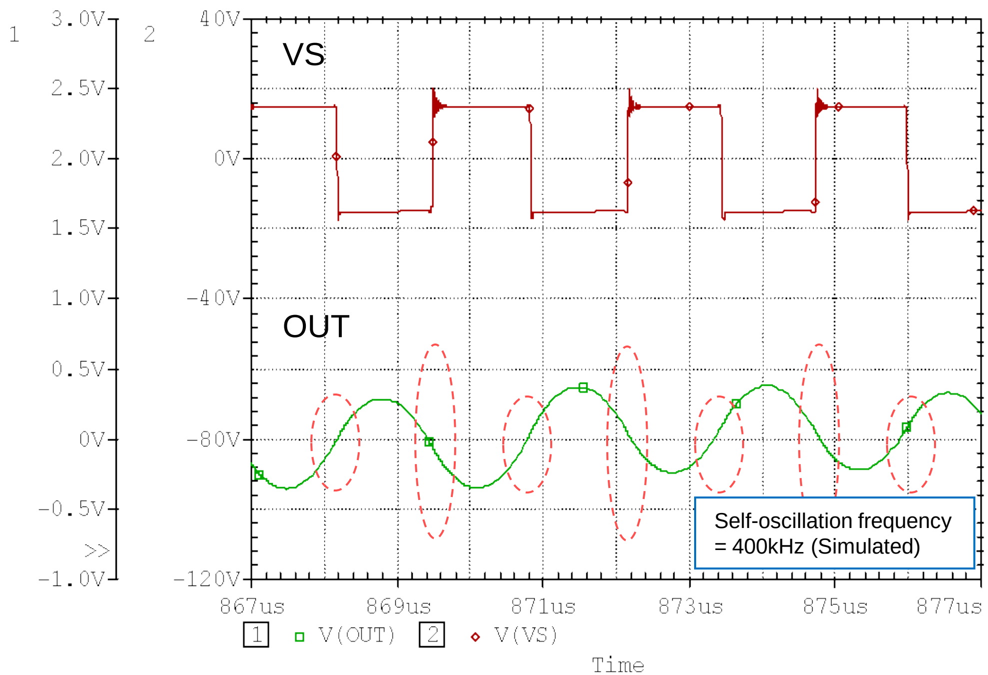
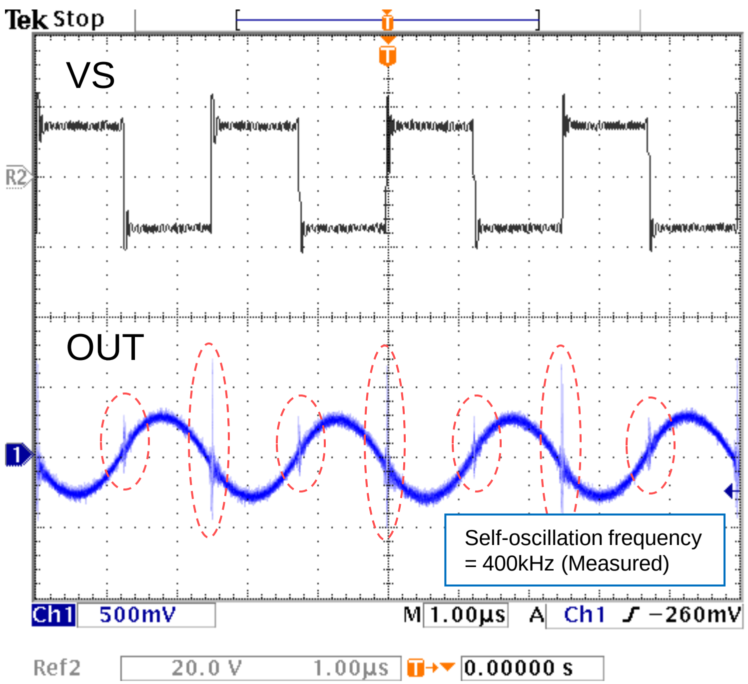
Simulation Result (without Capacitor Model)

Simulated (without output capacitor models)



Measured



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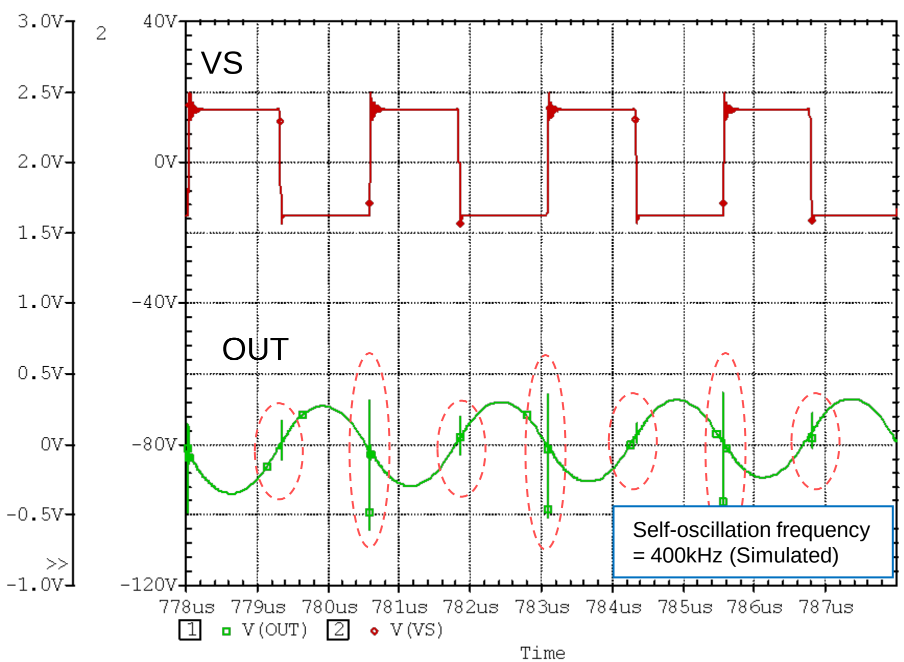
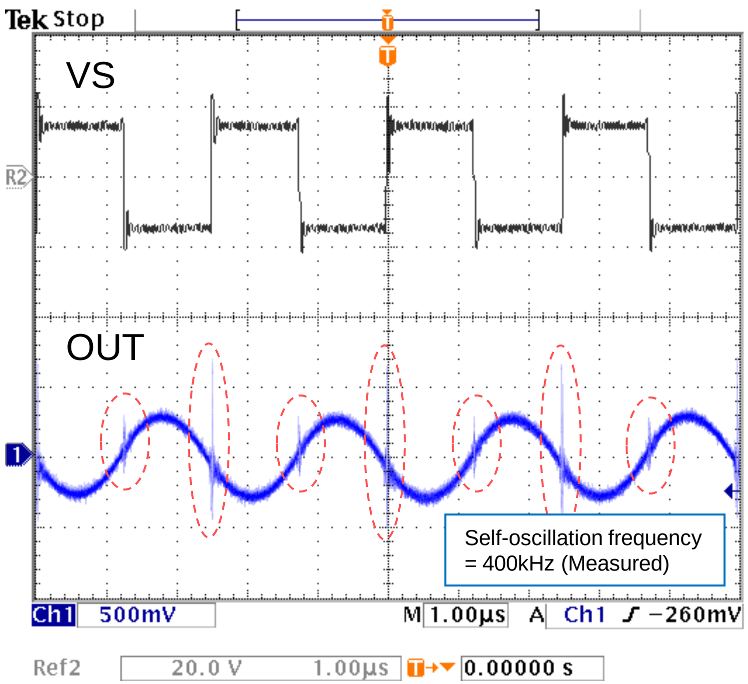
Simulation Result (with Capacitor Model)

Simulated (with output capacitor models)



Measured



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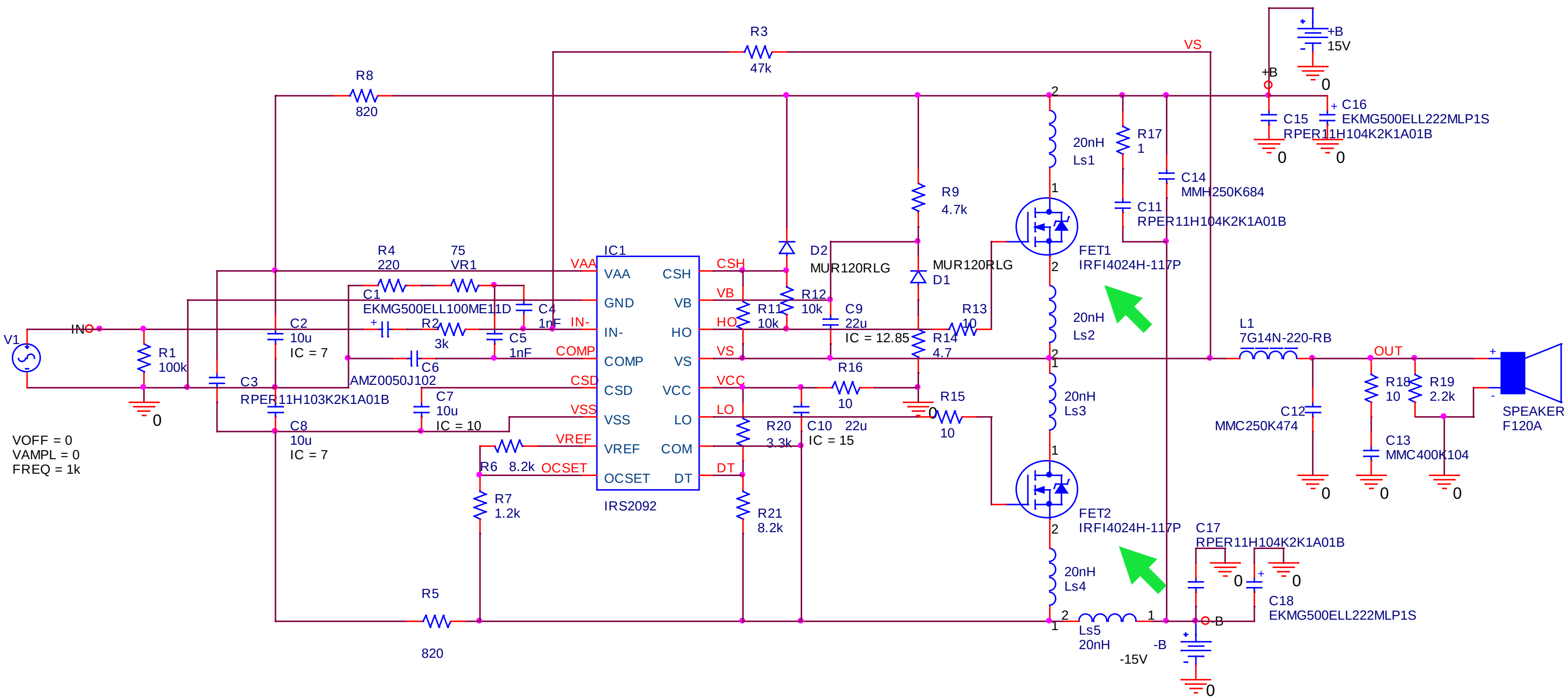
13. Simulated Performance of the circuit with different FETs

IRFIZ24N Key Parameters		
V_{DS}	55	V
I_D	14	A
$R_{DS(ON)}$ typ. @ 10V	70	mΩ
Q_g typ.	13.4	nC
t_{ON} typ.	38.9	ns
t_{OFF} typ.	46	ns
Q_{rr} typ.	120	nC

IRFI4024H-117P Key Parameters		
V_{DS}	55	V
I_D	11	A
$R_{DS(ON)}$ typ. @ 10V	48	mΩ
Q_g typ.	8.9	nC
t_{ON} typ.	7.9	ns
t_{OFF} typ.	16.4	ns
Q_{rr} typ.	11	nC

Simulated Performance of the circuit with different FETs



	IRFIZ24N	IRFI4024H-117P
Efficiency (@ 25W, 4Ω)	93.505%	94.578%
Distortion (@ 1kHz, 4Ω, 10W)	0.0144 %THD	0.0201 %THD

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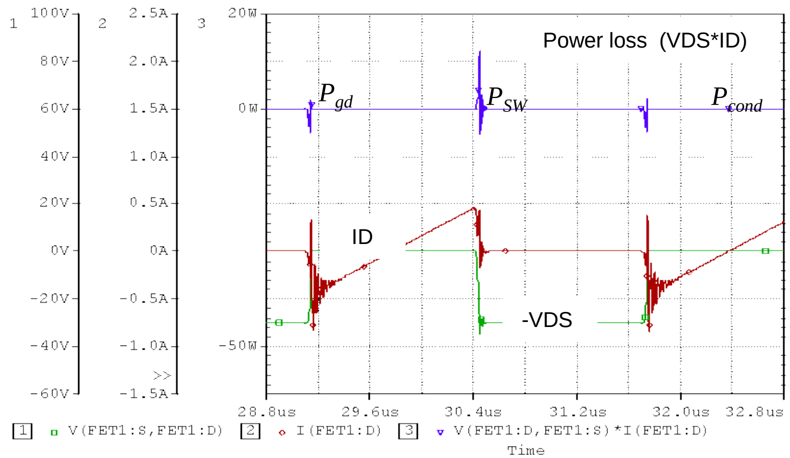
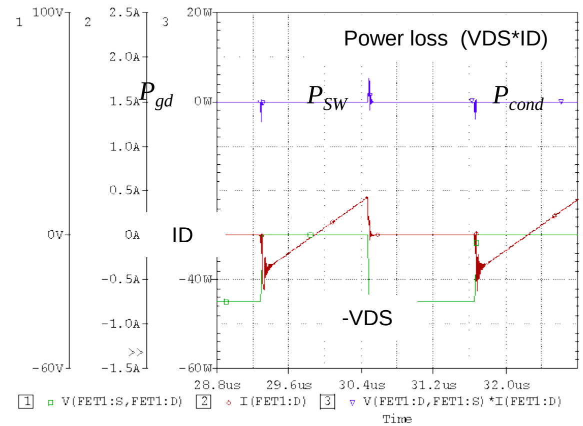
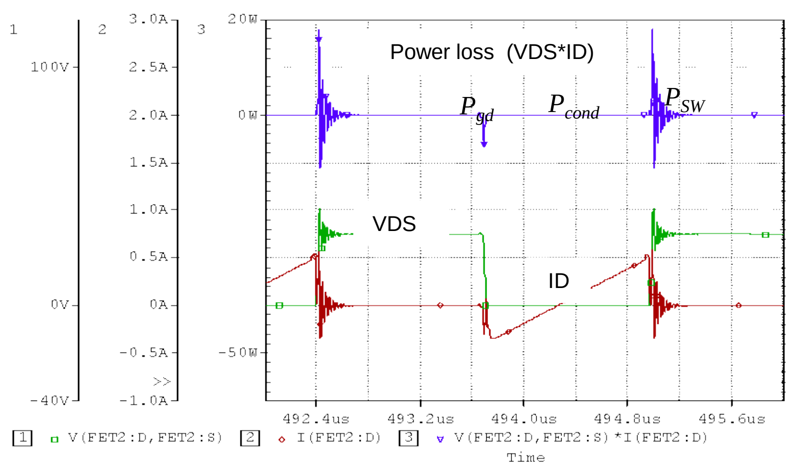
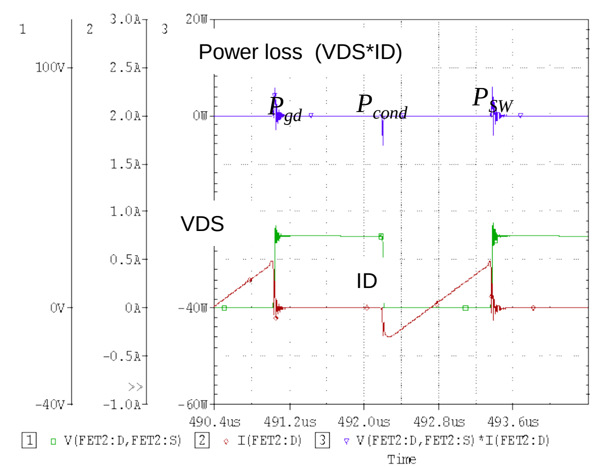
Simulated Performance of the circuit with different FETs

	IRFIZ24N	IRFI4024H-117P
FET1		
FET2		

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